

# **Sensor Analog IP Developments for IOT application**

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# About Me

- **Principal Analog Engineer, Renesas Electronics Dresden Germany, 2023 -**
  - Technical Lead, Fraunhofer IIS/EAS, 2018 - 2011
  - Principal Engineer/PL, SK Hynix Korea, 2013-2017
  - Scientist II, Institute of Microelectronics A\*STAR, Singapore, 2011-2013
  - Senior Engineer, System LSI, Samsung Electronics, Korea 2007 - 2011
  - Member of Research Staff, SAIT, Samsung Electronics, Korea, 2004-2011
- **Dr.-Ing., Electrical Engineering, Technische Universität München, Germany 2005**
  - Doktorand, Corporate Research, Infineon Tech. AG, Munich, Germany 2001 – 2004
  - Diplomand, Automotive & Industrial, Infineon Tech. AG, Munich, Germany 2000

# Today's talk

## 1. IOT ?

1.1 Components in IOT systems

1.2 IOT Player

1.3 IOT Market

## 2. Sensor Analog IP Developments for IOT

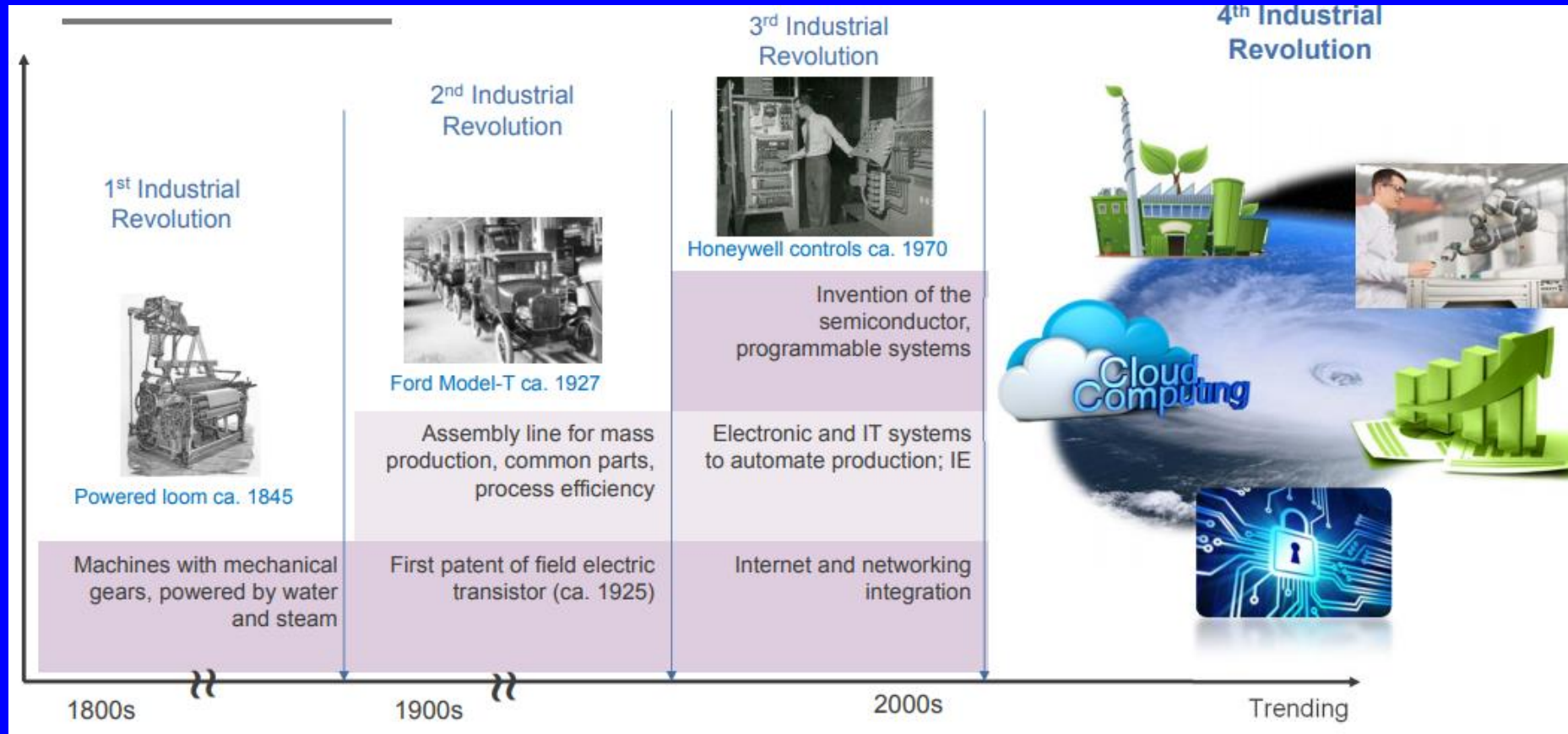
2.1 Sensor Analog IP Developments in PD-SOI

2.2 Sensor Analog IP Developments in FD-SOI

# 1. Internet of Things ?

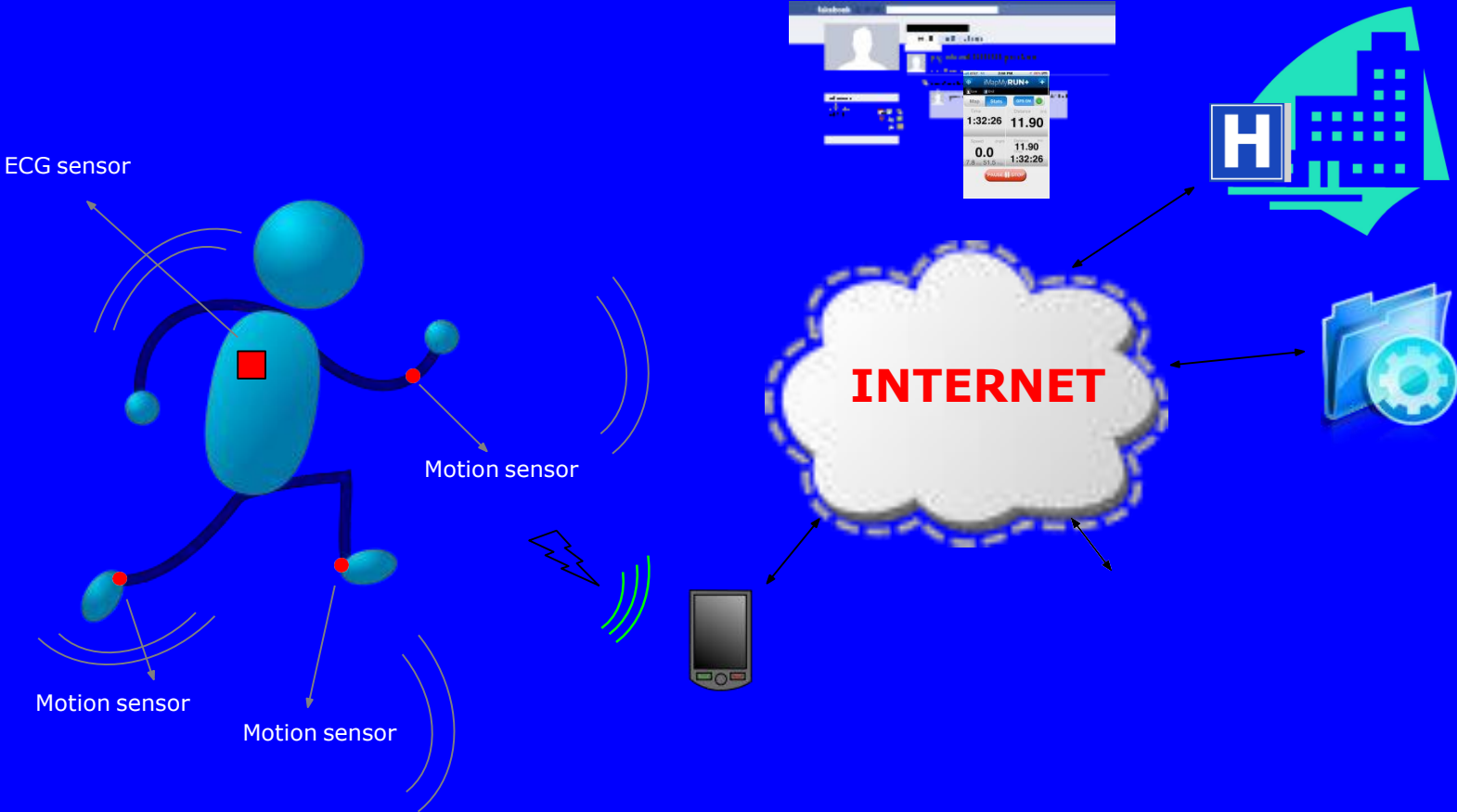
# Internet Of Things ??

- Industry 4.0



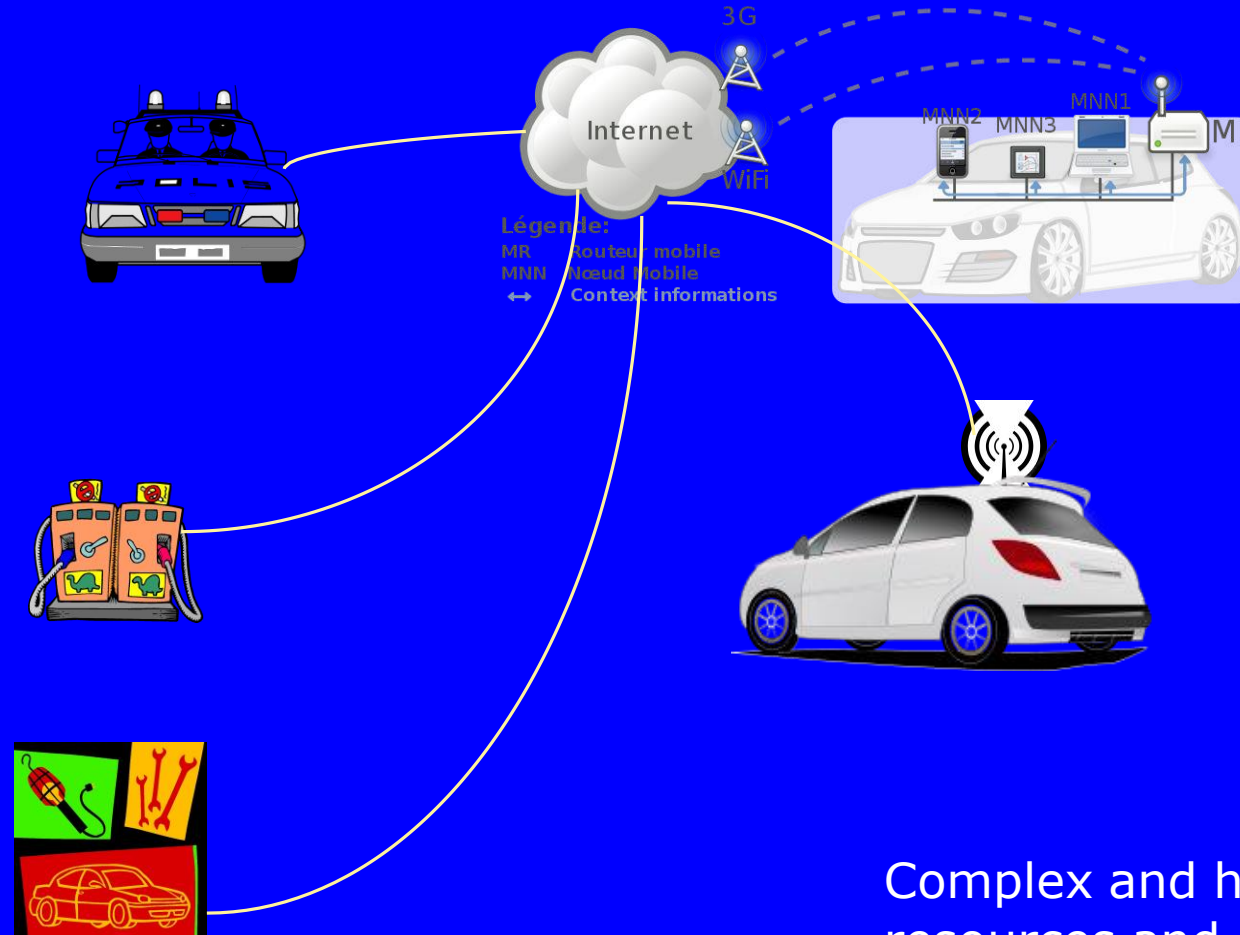
# Internet Of Things ??

- PEOPLE connecting to THINGS



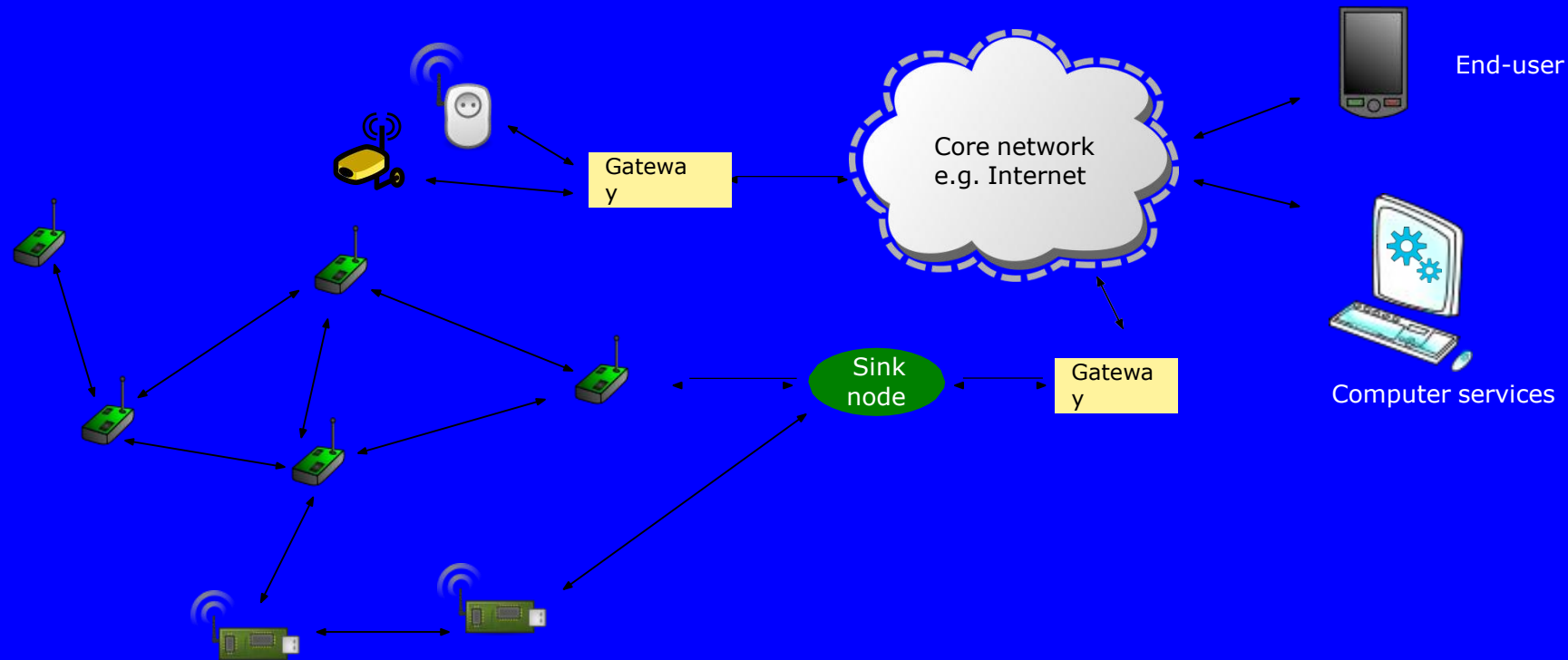
# Internet Of Things ??

- **THINGS** connecting to **THINGS**



# Internet Of Things ??

- Wireless Sensor Network



The networks typically run Low Power Devices  
Consist of one or more sensors, could be different  
type of sensors (or actuators)



# Internet Of Things ??

- More Things are connected

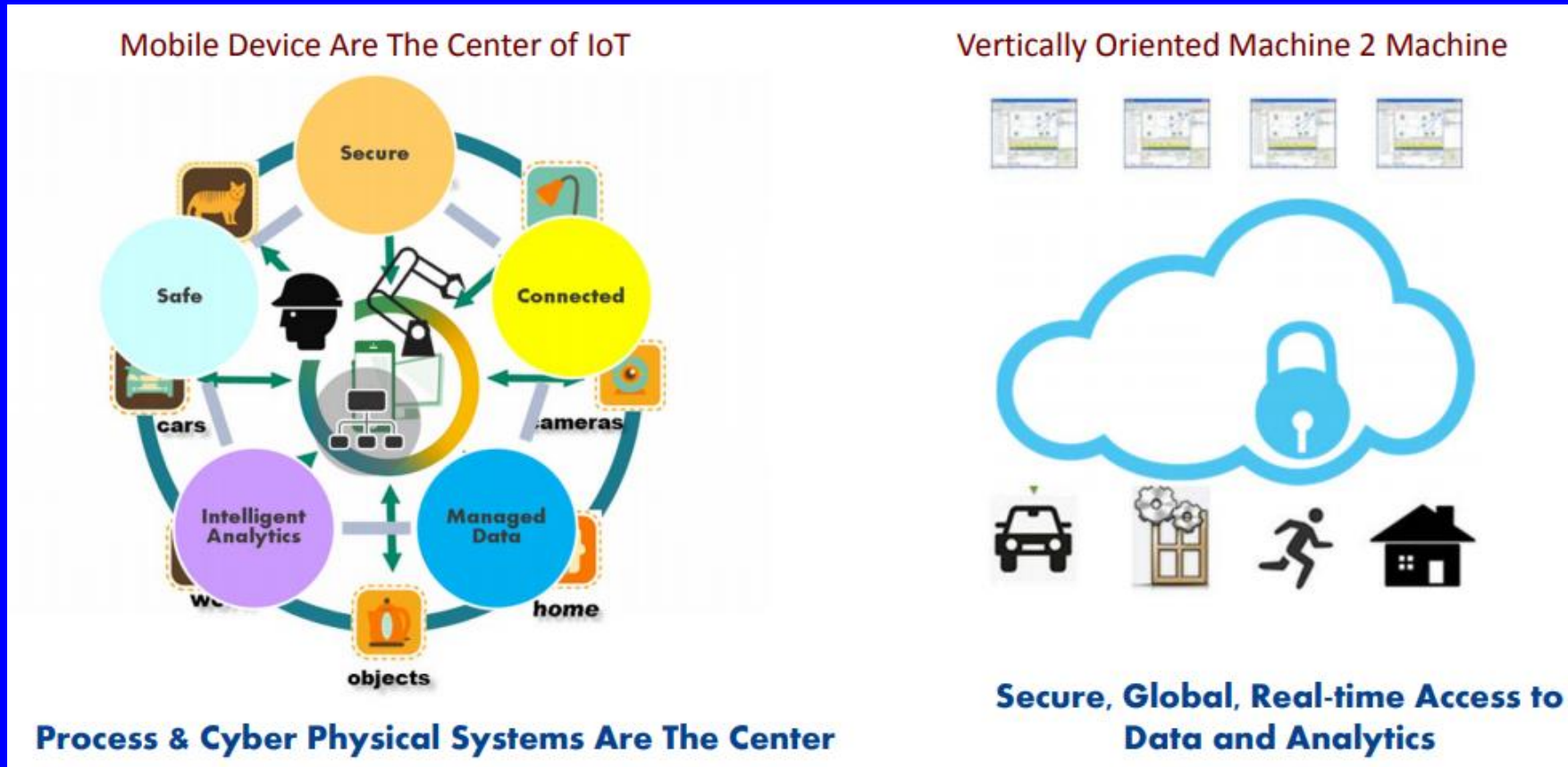
Home/daily-life  
devices Business and  
Public  
infrastructure  
Health-care

...



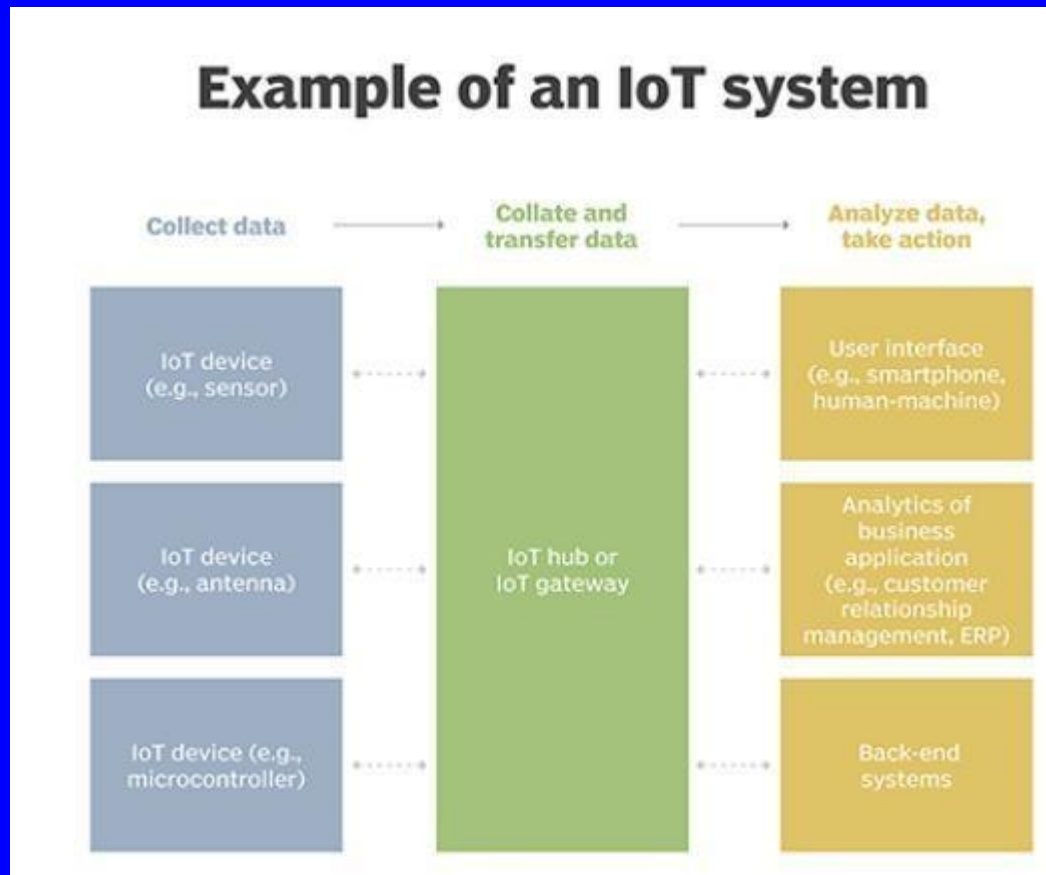
# Internet Of Things ??

- IoT keeps changing The Typical Definition



# Internet Of Things ??

- Examples of IOT systems



# NOW WE CAN SAY Internet Of Things

- The Internet of Things (IoT) is the network of physical objects or "things" embedded with electronics, software, sensors, and network connectivity, which enables these objects to collect and exchange data.
- IoT allows objects to be sensed and controlled remotely across existing network infrastructure, creating opportunities for more direct integration between the physical world and computer-based systems, and resulting in improved efficiency, accuracy and economic benefit.

# “SENSORS/ACTUATORS” in IOT systems

- **Sensors:**
  - They are mainly input components
  - They sense and collect surrounding information
- **Basically three types:**
  - Passive, omnidirectional (e.g. mic)
  - Passive, narrow-beam sensor (e.g. PIR)
  - Active sensors (e.g. sonar, radar, etc.)
- **Actuators:**
  - They are mainly output components
  - They alter the surrounding
- **Some examples:**
  - Adding lighting, heat, sound, etc.
  - Controlling motors to move objects
  - Displaying messages
  - and others...

# “THINGS” in IOT systems

- We can turn almost every object into a “thing”.
- A “thing” still looks much like an embedded system currently.
- **A “thing” generally consists of four main parts:**
  - **Sensors & actuators**
  - **Microcontroller**
  - **Communication unit**
  - **Power supply**
- A “thing” has the following properties:
  - It’s usually powered by battery. This implies limited source of energy.
  - It’s generally small in size and low in cost. This limits their computing capability.
  - It doesn’t usually perform complicated tasks.
- **Power consumption is the main design issue.**

# “COMMUNICATIONS” in IOT systems

- A “thing” always feature communications for “team working”
- The Role of Communications
  - Providing a data link between two nodes
- **Communication type:**
  - Wireline (e.g. copper wires, optical fibers)
  - Wireless (e.g. RF, IR). RF-based communication is the most popular choice (and also our focus)
- Popular RF-based communication solutions:
  - IEEE 802.15.4 □ used in XM1000
  - IEEE 802.11 (or Wifi)
  - Bluetooth
  - Near Field Communication (NFC), e.g. RFID
- **Main concern: Security, Reliability & Performance**

# “NETWORKS” in IOT systems

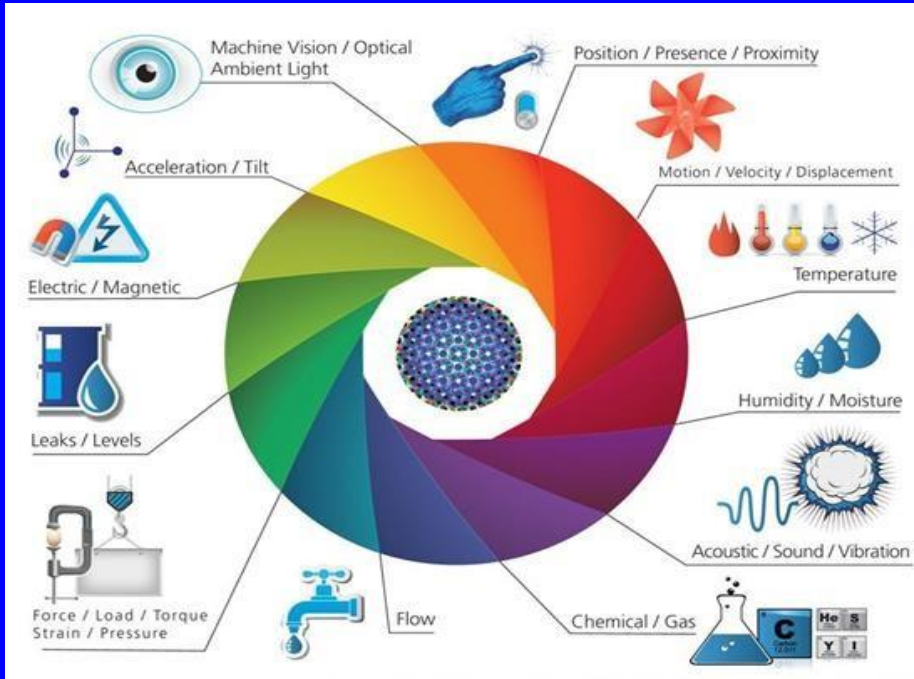
- **The Roles of Networks**
  - Managing nodes (discovery, join, leave, etc).
  - Relaying data packets from the source to the destination node in the network.
- **Networks are a distributed system. All nodes need to perform networking related tasks.**
- **RF-based Network in IoT is usually a Wireless Multi-hop Network. Some examples:**
  - **Wireless Sensor Networks (WSNs)**
  - **Mobile Wireless Ad hoc Networks (MANETs)**
  - **Wireless Mesh Networks (WMNs)**
  - **Vehicular Ad Hoc Networks (VANETs)**
  - **and others...**
- **Main concern: Security, Reliability & Performance**



# “THE INTERNET” in IOT systems

- **The Internet uses TCP/IP.**
  - This implies that things must also support TCP/IP.
  
- **Gateway (or sink)**
  - For a practical deployment, a gateway is often needed in a network.
  - It offers relaying packets between the network and the Internet.

# Examples of “SENSORS/ACTUATORS” in IOT systems



- By combining a set of sensors and a communication network, IoT devices share information with one another and are improving their effectiveness and functionality.”

# IOT Players

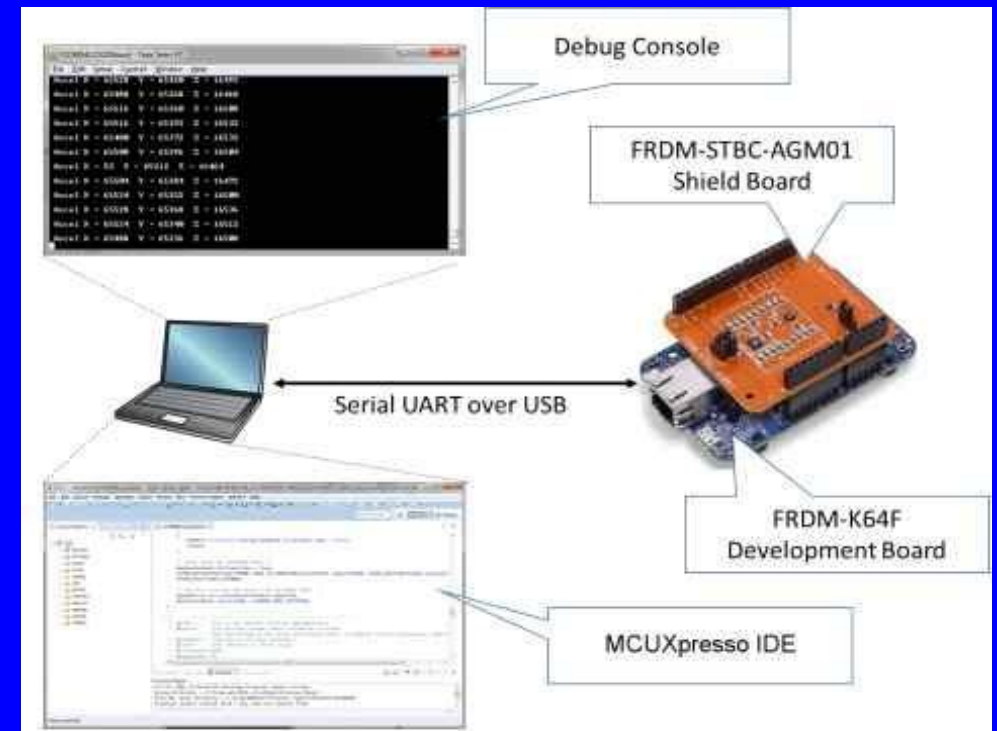
- **ST Microelectronics (France)**
  - Strong in MEMS sensor products
  - Produces MEMS sensor based Gyro, 3 axis accelerator sensor
  - Now expands those products with AI



Motion sensor (2.5x3x0.83 mm<sup>2</sup>)  
from STM

# IOT Players

- **NXP (The Netherlands)**
  - Strong in Sensor Products
  - Motion Sensor, Magnetic Sensor, Touch Sensor, Temperature Sensor etc
  - Announces ISSDK (IOT Sensing Software Development Kit)



ISSDK from NXP

# IOT Players

- **INFINEON (Germany)**
  - Strong in Automotive Products
  - Very active in Lidar Sensor (ADAS)
  - Announces XENSIV for multi sensor applications



Lidar Sensor from Infineon

# IOT Players

- **BOSCH (Germany)**
  - Strong in MEMS Process/Products
  - Bosch Sensortec (Dresden) provides mobile sensor products
  - Bosch (Reutlingen) provides Automotive/Industrial sensor products



MEMS Sensor from Bosch

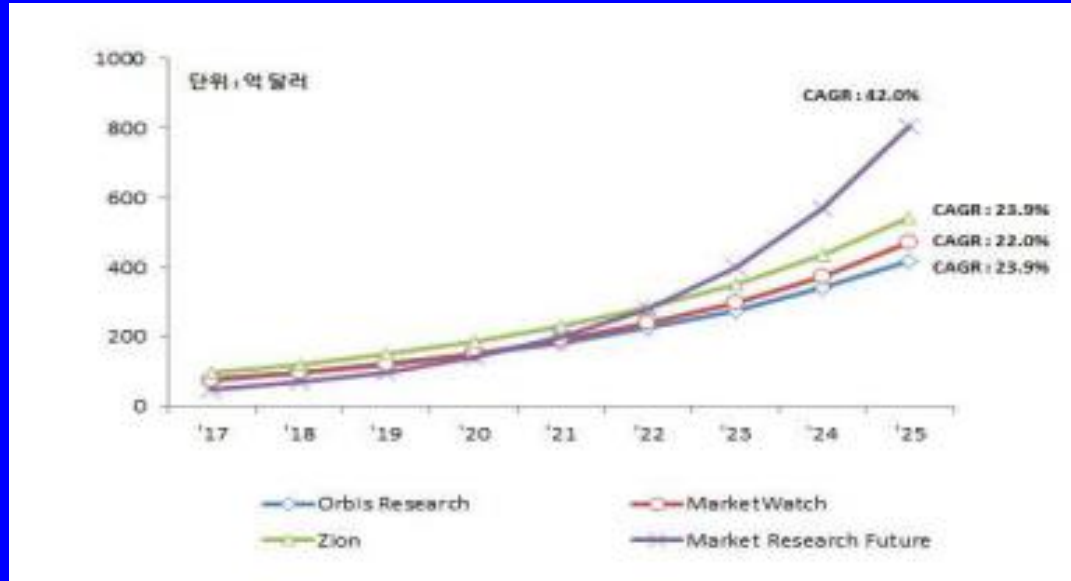
# IOT Players

- **RENESAS ELECTRONICS (Japan)**
  - Strong in MCU, Automotive
  - Expands products for Industrial IOT application



Industrial IOT Sensor from Renesas

# IOT Market



IOT Sensor Market Volume Size  
From Gartner

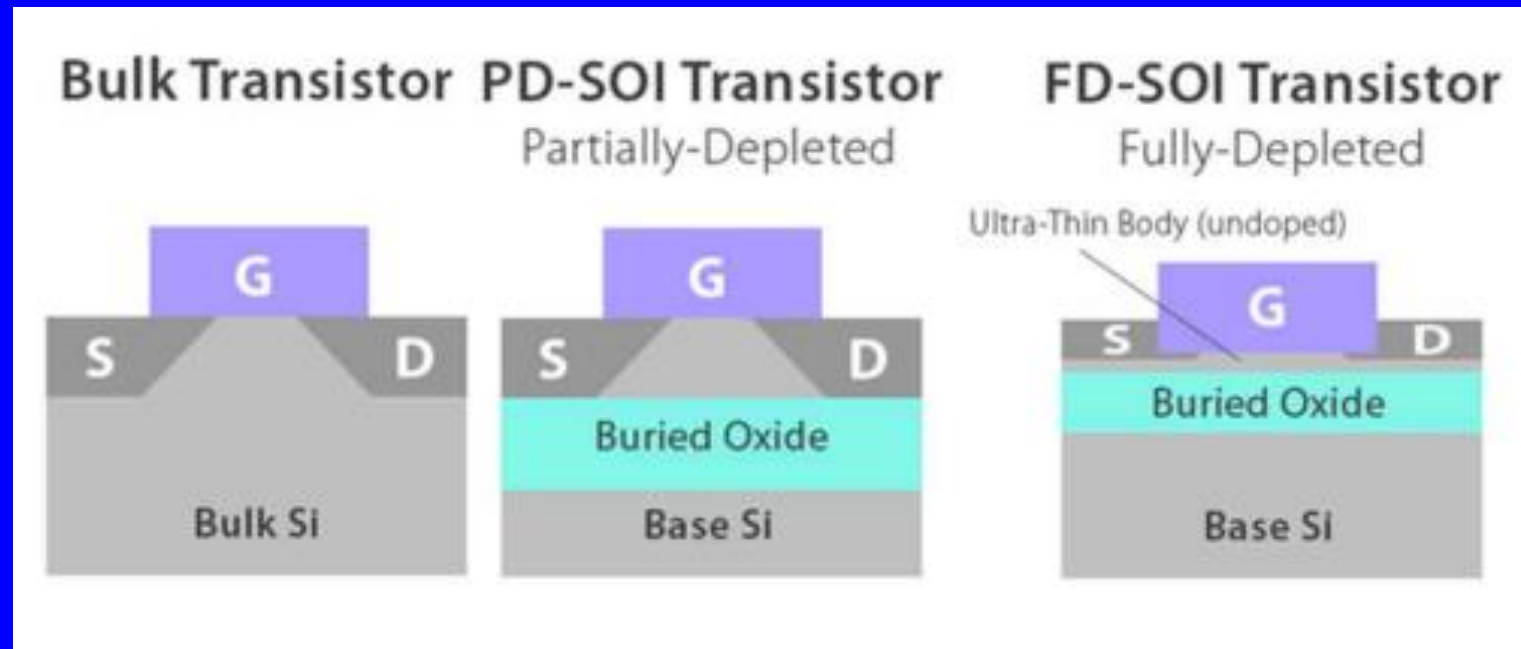


IOT Sensor Market Share by Region  
From Marketand (2018)



## **2. Sensor Analog IP Developments for IOT**

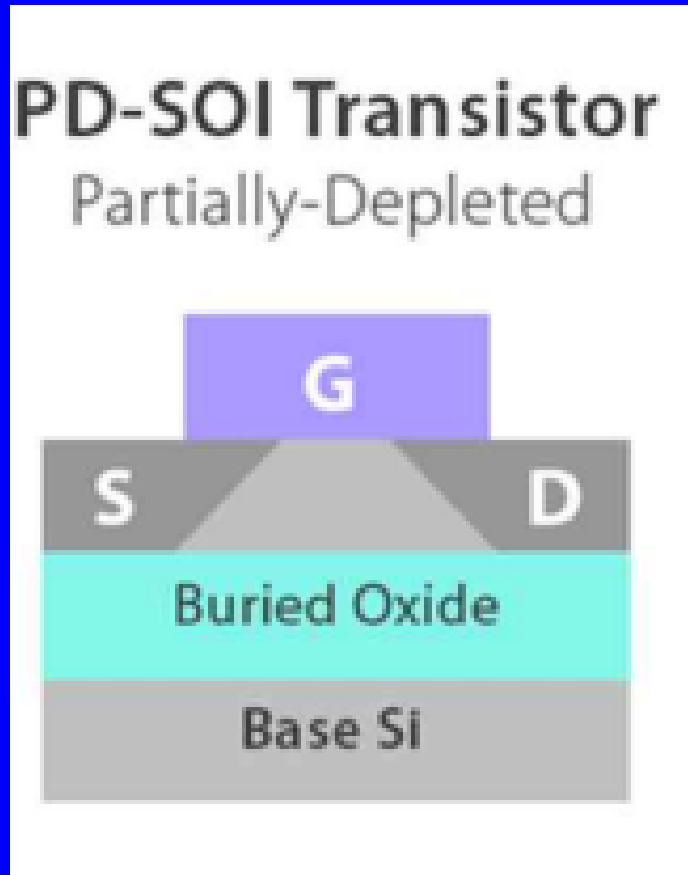
# SOI process



- **What are PD-SOI and FD-SOI?**

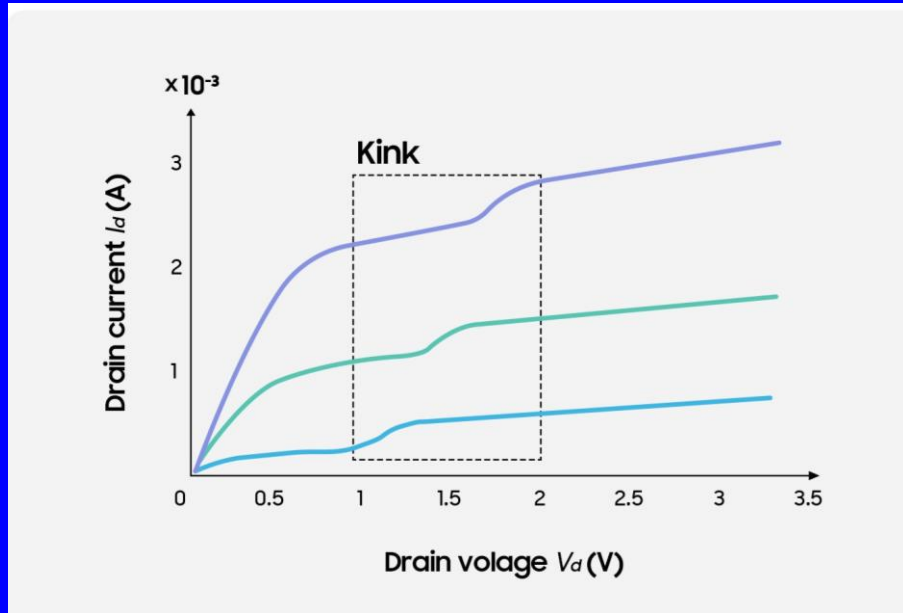
- Partially Depleted SOI (PD-SOI) and Fully Depleted SOI (FD-SOI), based on the thickness of the Buried Oxide Layer (BOX) and the thickness of the monocrystalline silicon for the channels.

# PD-SOI process



- **PD-SOI process pros** PD-SOI is applied to analog products such as power devices, with the thickness of the monocrystalline silicon for the channel ranging from 50nm-100nm, and the thickness of the BOX ranging from 100-200nm.
  - PD-SOI has the **advantage** of **blocking leakage** current through the junction when compared to bulk transistors, and it also **reduces the capacitance** generated between the source, drain and body.

# PD-SOI process

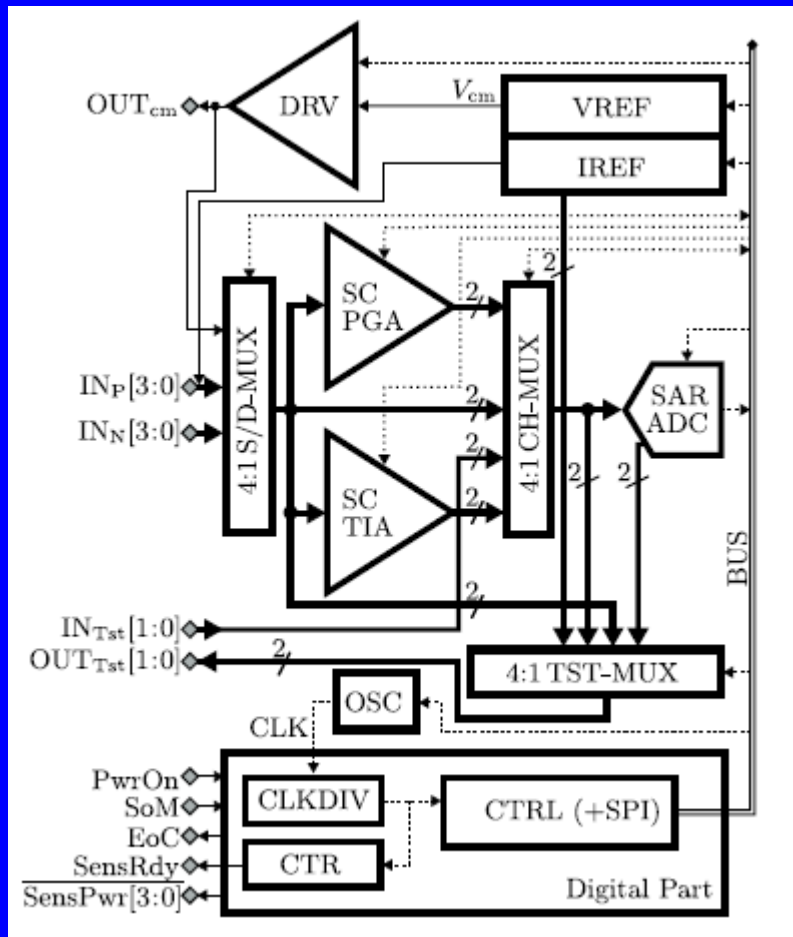


- **PD-SOI cons**

- No/not enough body contacts causes a floating body effect.
- Floating body effect cause threshold voltage ( $V_{th}$ ) variation of the device, resulting in an increased off current when the device is turned off, with a kink effect occurring when the drain current suddenly increases from the point where the  $V_{th}$  is lowered.

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# Multi-Channel Sensor Analog-Frontend for IOT



Ultra-low power analog sensor frontend (AFE) for IOT are developed in a PD-SOI 180 nm process

- The flexible channel-wise configuration enables processing of various signal types and therefore offers a versatile solution for sensors from the Internet-of-Things (IoT) market segment.
- Four input channels are separately configurable to process voltage, current and potentiometric signals of external or internal sources.
- Resolution (6 bit to 13 bit), sample rate (1 to 7.5 kS/s), voltage gain (-6 to 12 dB), transimpedance (1.5 M $\Omega$  to 12 M $\Omega$ ) are programmable
- Fabricated samples in PD-SOI180 nm technology show an ultra-low power consumption of **8.8 $\mu$ W**.
- Specifically, the **SARADC** achieves 10.6 effective bits while consuming 1.8 $\mu$ W, resulting in a Figure-of-Merit of 116.0 fJ/conv.-step

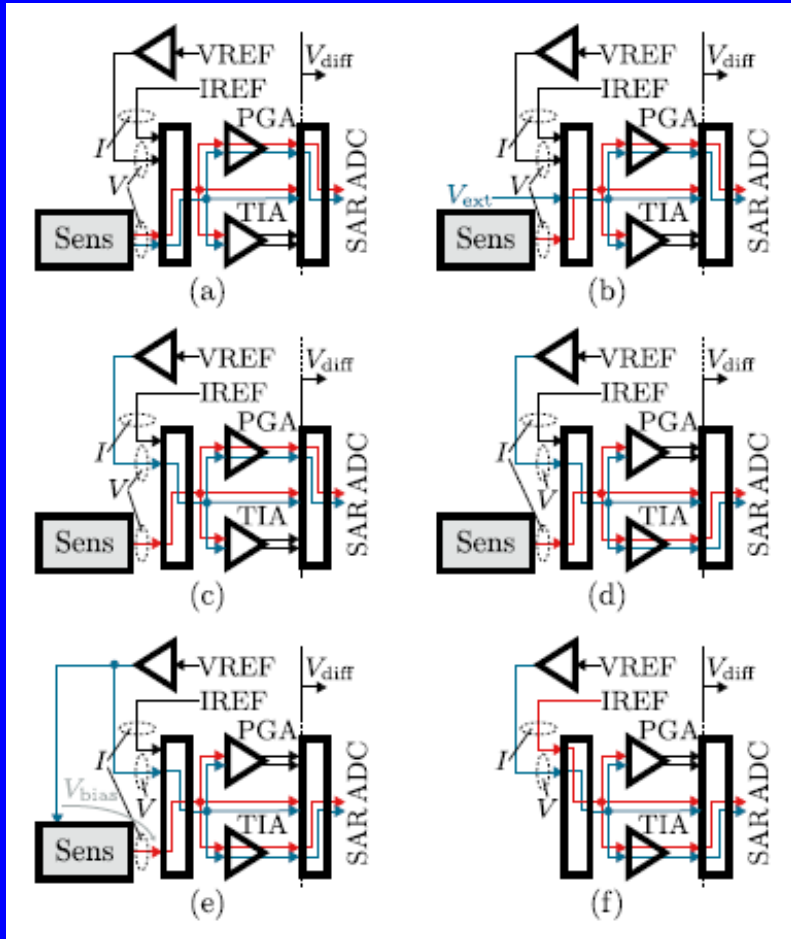
# Multi-Channel Analog-Frontend for IOT

- Design Targets are derived based on industry requirements through the survey.

1	Temperature	MAXIM	MAX6607 <sup>1</sup>	-20 °C to +85 °C	Voltage: 0.2 V to 1.4 V	below 1 Hz	8 μA to 15 μA
2	Ambient Light	Renesas	ISL1902 <sup>1</sup>	0.3 lux to 10 klux	Voltage: 0.02 V to Supply	below 5 kHz	0.65 μA to 15 μA
3	CO Gas	Spec Sensors	3SP_CO <sup>1</sup>	0 ppm to 1000 ppm	Potentiometric Current: 0 A to 26 μA	below 1 Hz	10 μW to 50 μW
4	Accoustic	PUI Audio	PMM3738	more than 100 Hz	Voltage: 0 V to Supply	more than 100 Hz	5 μA to 85 μA
5	Acceleration	Analog Devices	ADXL316	±16 g to ±19 g	Voltage: 0.1 V to 75% Supply	below 1.6 kHz	250 μA to 400 μA
6	Humidity	Honeywell	HIH5030	0 %RH to 100 %RH	Voltage: 0.5 V to Supply	below 5 kHz	200 μA to 500 μA

- Survey of commercially available, IoT-compatible sensors with current consumption below 300 μA.

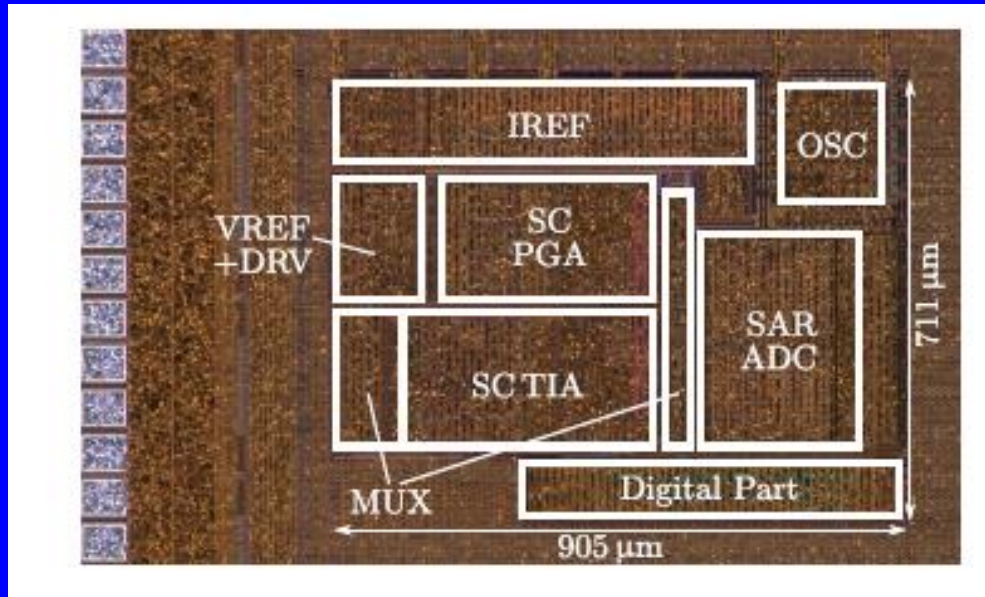
# Multi-Channel Sensor Analog-Frontend for IOT



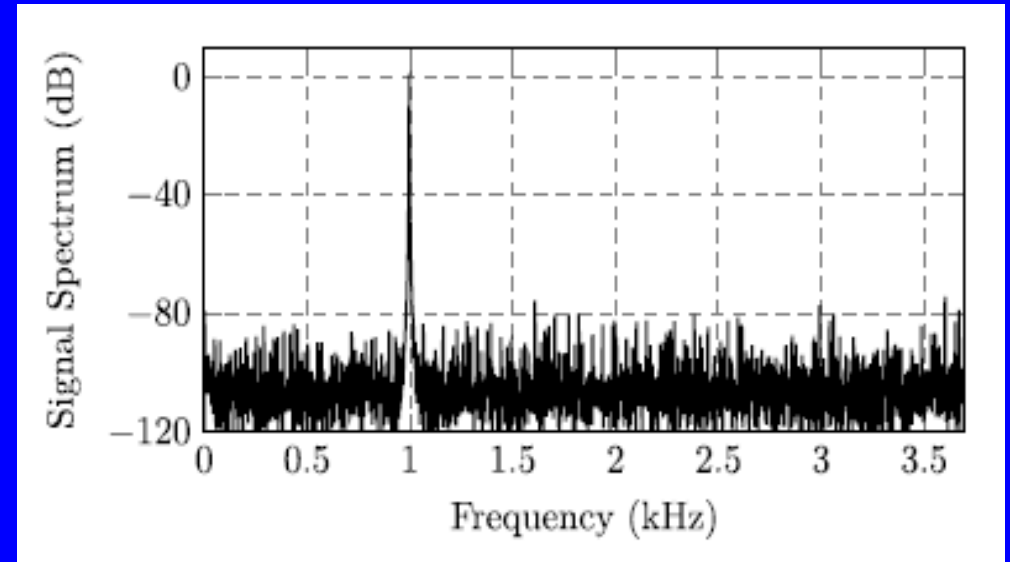
The Sensor supports 6 operation modes.

- (a) differential voltage
- (b) single-ended voltage with external reference
- (c) single-ended voltage with internal reference
- (d) single-ended current with internal reference
- (e) potentiometric current with internal reference
- (f) temperature monitoring

# Multi-Channel Sensor Analog-Frontend for IOT



- The total active area : 0.64mm<sup>2</sup>
- Analog parts: SARADC (14.9%), PGA (23.8%), TIA (14.9%) and current reference (15.6%)
- Digital parts : 9%



- The output spectrum is obtained with FFT with 1 kHz input.
- The peak differential ENOB : 10.6 bit

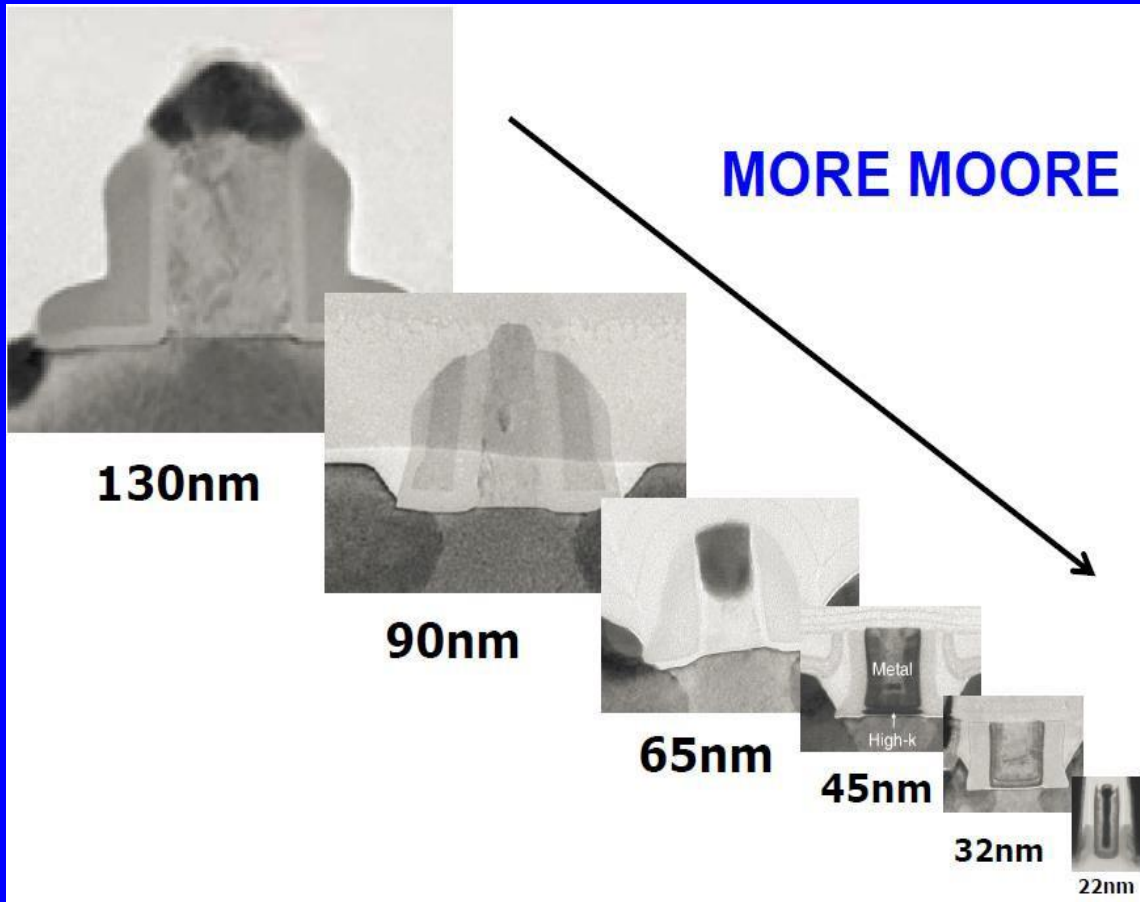


# Multi-Channel Sensor Analog-Frontend for IOT

	This Work, 2021	[9], 2021	[10], 2020	[13], 2019	[6], 2019	[8], 2018	[17], 2017	[7], 2017
<b>General</b>								
Analog Supply (V)	1.8	1.8	2	0.6	1	0.6	1.2	0.3
Tech. (nm)	180	180	130	65	180	40	65	65
Application	IoT	IoT	Bio	IoT	Bio	Bio	Bio	Bio
Total Sample Rate (kS/s)	1 to 7.5	0.1	1	10 to 100	N/A	20 to 400	0.4	1.0
Total Bandwidth (kHz)	0.01 to 3.8	0.0001 to 0.05	0.04 to 0.32	N/A	N/A	0.001 to 128	N/A	0.02 to 0.42
Area (mm <sup>2</sup> )	0.64	1.81	0.6	0.08	0.23	1	0.13 <sup>2</sup>	0.22
Average Power (μW)	1.8 <sup>2</sup> / 8.8	160.5 <sup>2</sup> / 425 to 500	1.3 <sup>2</sup> / 6.3	0.0003 to 0.6	2 <sup>2</sup> / 5.4	0.24 <sup>2</sup> / 3.8	0.1 <sup>2</sup>	0.0038
Support commercial IoT sensors? (e. g. Table I)	Yes	Yes <sup>3</sup>	No <sup>4</sup>	No <sup>4</sup>	No <sup>4</sup>	No <sup>4</sup>	No <sup>4</sup>	No <sup>4</sup>
<b>ADC</b>								
ADC Sample rate (kS/s)	1.25 to 10	N/A	1	10 to 100	N/A	20 to 400	0.4	1.0
Resolution (bit)	6 to 13	SAR: 8 to 12	8	10	N/A	13	10	8
ENOB (bit)	10.6	8.5 to 12.9	7.9	N/A	7	9.7	9.6	7
FoM <sub>ADC</sub> (fJ/st.)	116.0	N/A	5.2e3	31 to 150	14.4	322.0	15.6	34.8
<b>Preamplifier</b>								
Prog. Gain?	Yes	No	Yes	No	Yes	Yes	N/A	No
Gain (dB)	-6 to 12	N/A	43 to 55	N/A	N/A	20 to 30	N/A	40
Preamp Power (μW)	3.9	28.6 to 107.8	1.6	N/A	N/A	N/A	N/A	0.0009

<sup>2</sup> stand-alone ADC excluding preamplifier      <sup>3</sup> electrochemical sensors and chemo-resistive sensors      <sup>4</sup> Table I bandwidth and/or voltage range not achieved

# Moore's law



How leading semiconductor manufacturer keeps pace with Moore's law?

- “Doubling of number of transistors per chip every 2 years” lowers cost per transistor → scaling 0.7 size every 2 years
- Performance improvement with scaling → advent of non-planar devices

Transistor size becoming smaller

# ITRS Roadmap

Table 4-1. RF and analog/mixed-signal CMOS technology requirements according to the ITRS roadmap, 2005 edition (see <http://www.itrs.net>).

Year of production	2005	2007	2010	2013	2016	2020
DRAM $\frac{1}{2}$ pitch <sup>(a)</sup> (nm)	80	65	45	32	22	14
(Technology node)						
Supply voltage <sup>(b)</sup> (V)	1.2	1.2	1.1	1.0	1.0	1.0
Gate length <sup>(c)</sup> (nm)	75	53	32	22	16	11
$t_{EOT}$ <sup>(d)</sup> (nm)	2.2	2.0	1.5	1.3	1.1	0.9
$1/f$ noise <sup>(e)</sup> ( $\mu\text{V}^2 \cdot \mu\text{m}^2/\text{Hz}$ )	190	160	90	70	50	30
$g_m/g_{ds}$ at $5 \cdot L_{min}$ digital <sup>(f)</sup>	47	32	30	30	30	30
$\sigma V_T$ matching <sup>(g)</sup> (mV $\cdot\mu\text{m}$ )	6	6	5	5	4	3
Peak $f_T$ <sup>(h)</sup> (GHz)	120	170	280	400	550	790
Peak $f_{max}$ <sup>(i)</sup> (GHz)	200	270	420	590	790	1110
NF <sub>min</sub> <sup>(i)</sup> (dB)	0.33	0.25	<0.2	<0.2	<0.2	<0.2

Source from ITRS2004

## International Technology Roadmap for Semiconductors

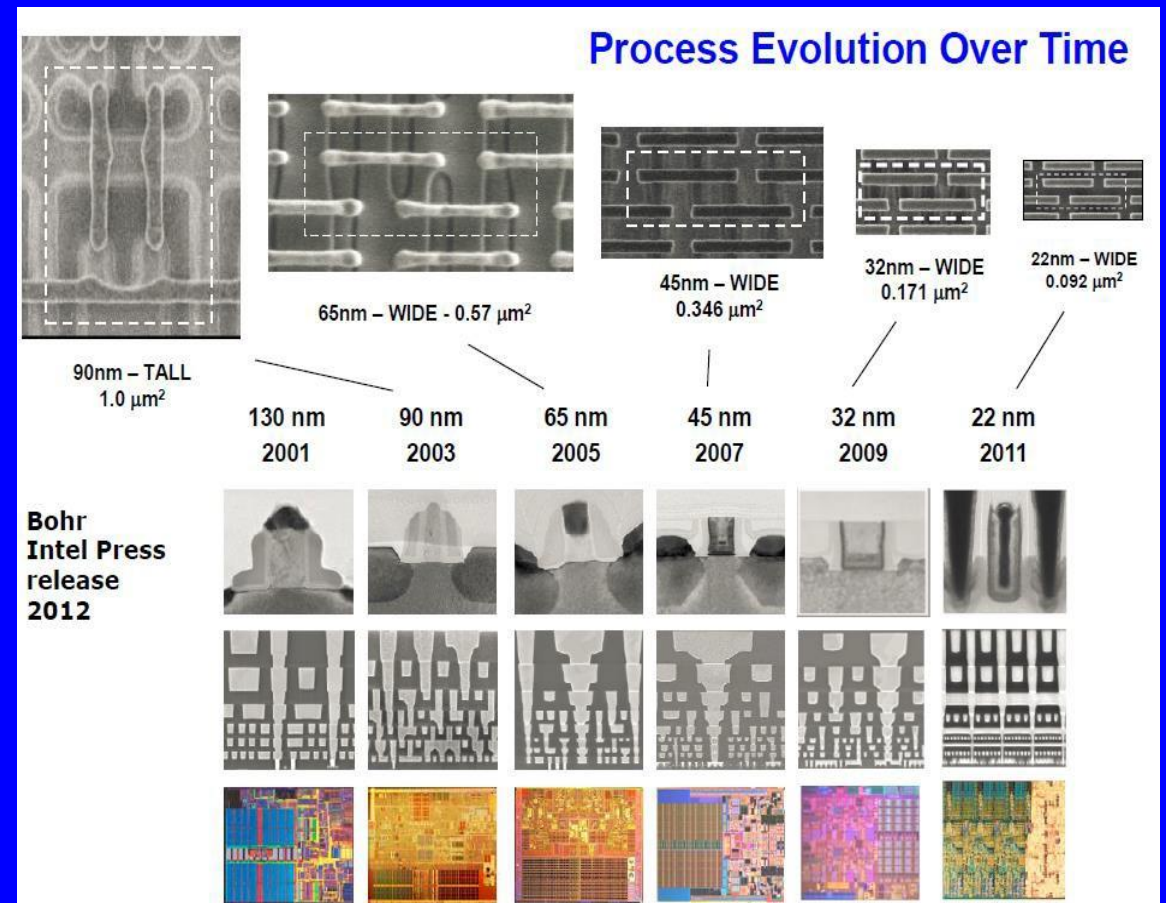
- The International Technology Roadmap for Semiconductors (ITRS) is a set of documents produced by a group of semiconductor industry experts. These experts are representative of the sponsoring organizations which include the Semiconductor Industry Associations of Taiwan, South Korea, the United States, Europe, Japan, and China. As of 2017, ITRS is no longer being updated. Its successor is the International Roadmap for Devices and Systems.
- International Roadmap for Devices and Systems (IRDS) assess present status and future evolution of the ecosystem in their specific field of expertise and produce a 15-year roadmap.
- IRDS reports includes evolution, key challenges, major roadblocks, and possible solutions.

# CMOS Technology Scaling/Evolution

## The International Technology Roadmap for Semiconductors

Table ITR01 - More Moore Device Technology Roadmap

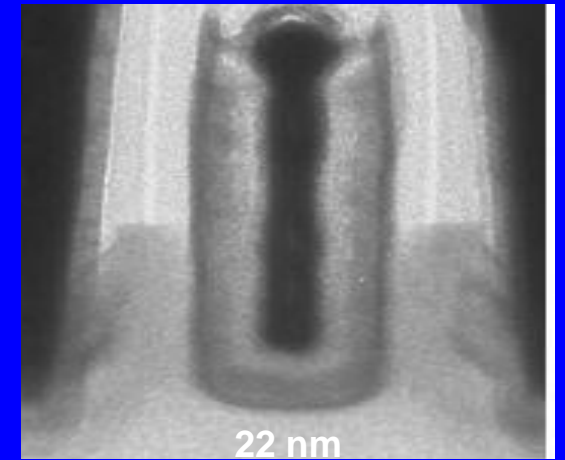
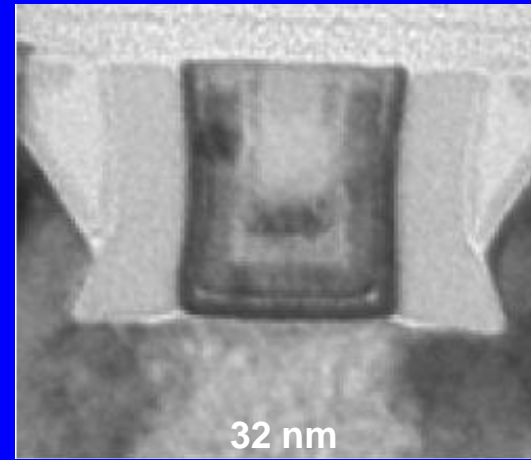
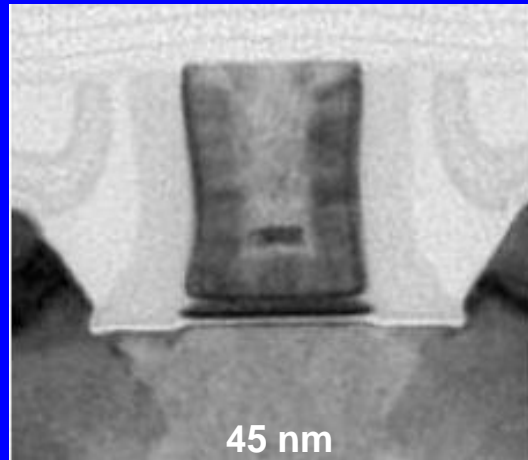
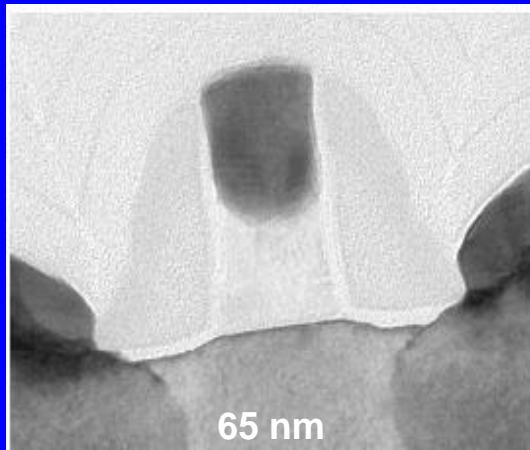
YEAR OF PRODUCTION	2015	2016	2018	2020	2022	2024	2026	2028
Logic device technology naming	P70M52	P52M36	P42M24	P32M16	P24M12	P24M12V1	P24M12V2	P24M12V3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"	"1/0.75"
Node production years	3	3	3	3	3	3	3	>3
Device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D	VGAA, M3D
<b>DEVICE ARCHITECTURE &amp; MODULES</b>								
Starting substrate	Si, SOI	Si, SOI	Si, SOI, SRB, QW	Si, SOI, SRB, QW	Si, SOI, SRB, QW	Si, SOI, SRB, QW	Si, SOI, SRB, QW	Si, SOI, SRB, QW
N-channel	Si	sSi	sSi, Ge	sSi, sGe, III-V	sSi, sGe, III-V	sSi, sGe, III-V	sSi, sGe, III-V	sSi, sGe, III-V
P-channel	Si	Si, SiGe	Si, SiGe	Si, SiGe	Ge	Ge	Ge	Ge
Channel formation	Etch	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI
Contact material	Silicide	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH
Contact integration	EPI	EPI	EPI WAC	EPI WAC	EPI WAC	EPI WAC	EPI WAC	EPI WAC
<b>DEVICE PERFORMANCE BOOSTERS</b>								
Main performance booster	SCE finHeight Vt	SCE finHeight Vt	Parasitics finHeight	Parasitics finHeight	Low Vdd 3D	Low Vdd 3D	Low Vdd 3D	Low Vdd 3D
Scaling focus	Perf	Power	Power	Power	Function	Function	Function	Function
Channel strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
S/D strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transport scheme	DD	Quasi Ballistic	Quasi Ballistic	Ballistic	Ballistic TFET, JFET, NCMOS	Ballistic TFET, JFET, NCMOS	Ballistic TFET, JFET, NCMOS, Spin	Ballistic TFET, JFET, NCMOS, Spin



source from Intel Corporation

# Scaling Focus

Source from Bai, Mistry, Natarajan, Auth IEDM/VLSI, 2004/7/8/12



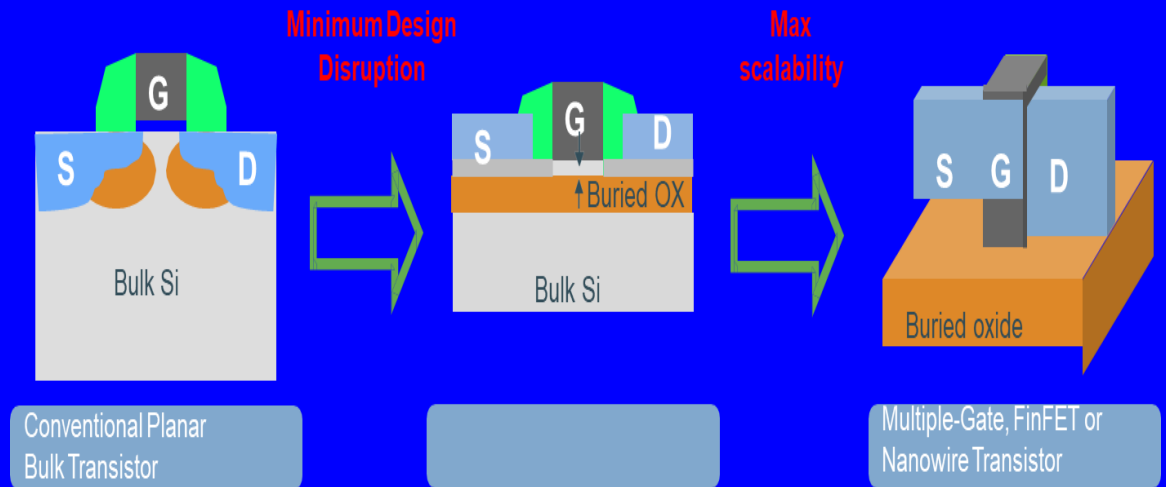
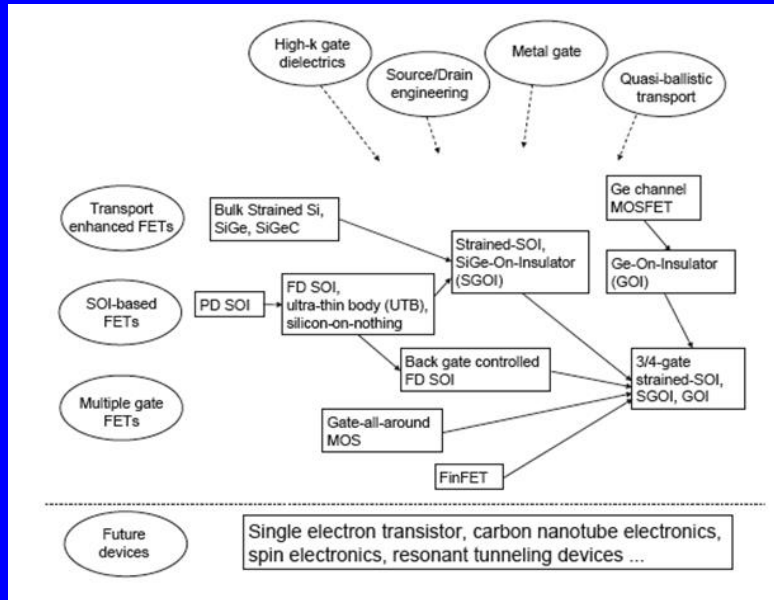
## Scaling – Before

- Scaling drove down cost
- Scaling drove performance
- Performance constrained
- Active power dominates
- Independent design-process

## Scaling - Now

- Scaling drives down cost
- Materials drive performance
- Power constrained
- Standby power dominates
- Collaborative design-process

# Planar FDSOI or Multi-Gate Transistor



## Multiple Device Architecture

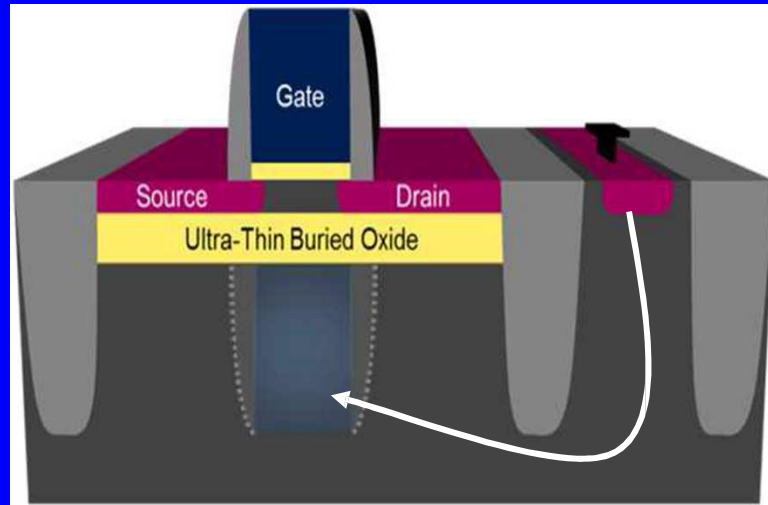
- A multitude of different approaches to enhance the performance of CMOS devices (in order for them to meet the ITRS requirements)

## FD-SOI

- Thin channel (Fully Depleted) with multi gates for better gate or short channel (SCE) control
- Better gate control → better transistors scaling

# FD-SOI Transistor Advantages

Source: GF 22FDX™ Platform



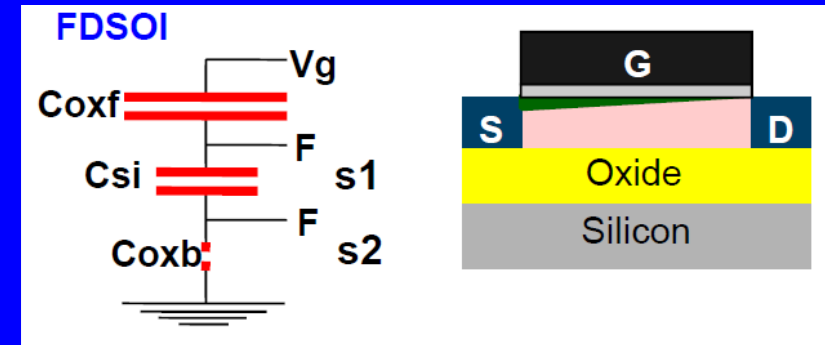
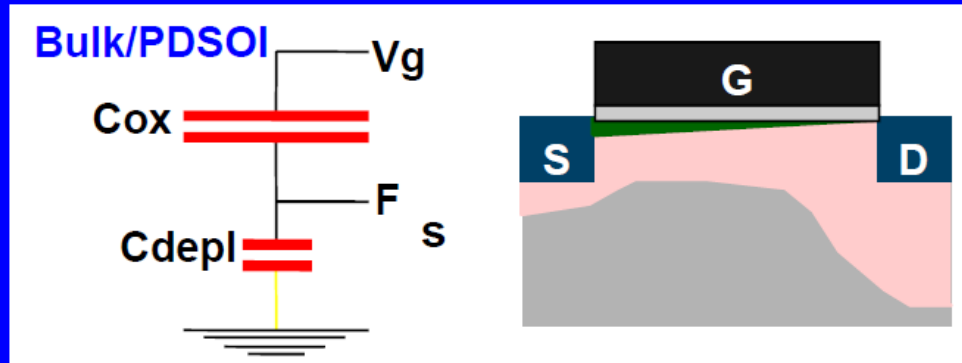
## Knobs to control Performance/Power:

- Gate bias
- Back Bias

UTBB FDSOI Transistor Advantages	
Total dielectric isolation	<ul style="list-style-type: none"><li>• Lower S/D capacitances</li><li>• Lower S/D leakage</li><li>• Latch-up immunity</li></ul>
Ultra thin Body	<ul style="list-style-type: none"><li>• Excellent SCE (SS, DIBL)</li><li>• No History Effect</li><li>• Lower SER</li></ul>
No channel doping	<ul style="list-style-type: none"><li>• Improved <math>V_T</math> variability</li><li>• Improved mismatch (SRAM &amp; analog)</li><li>• Better analog gain</li><li>• Reduced process cost</li></ul>
Ultra thin BOX option	<ul style="list-style-type: none"><li>• Enables Extended body biasing</li></ul>
Channel mobility boost	<ul style="list-style-type: none"><li>• Scalable down to 10nm</li></ul>
Conventional planar processing	<ul style="list-style-type: none"><li>• Lower manufacturing risk</li><li>• Equivalent bulk design</li></ul>

# FDSOI Device Physics

Source: GF 22FDX™ Platform



## FDSOI shows better performance compared to Bulk Transistor

- Body factor:  $n = \dots 1.05 \dots$  in FDSOI;  $\dots 1.5 \dots$  in Bulk

Linear current:  $I_D = \mu C_{ox} \frac{W}{L} \left( (V_G - V_{TH}) V_D - \frac{1}{2} n V_D^2 \right)$

Saturation current:  $I_{Dsat} = \frac{1}{2n} \mu C_{ox} \frac{W}{L} \left( (V_G - V_{TH})^2 \right)$

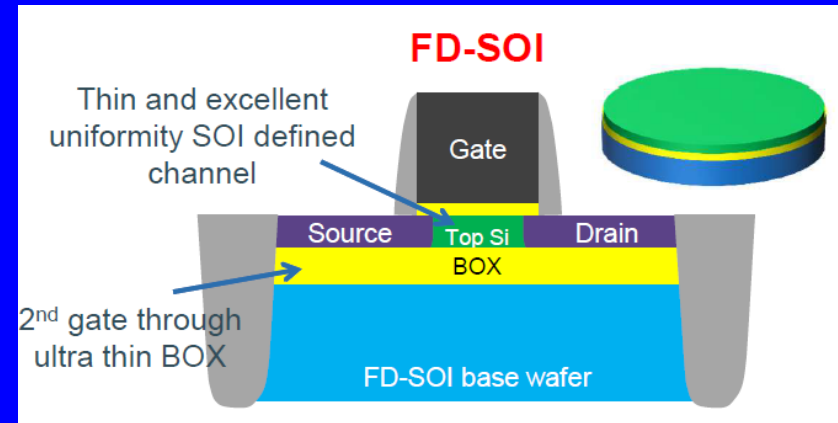
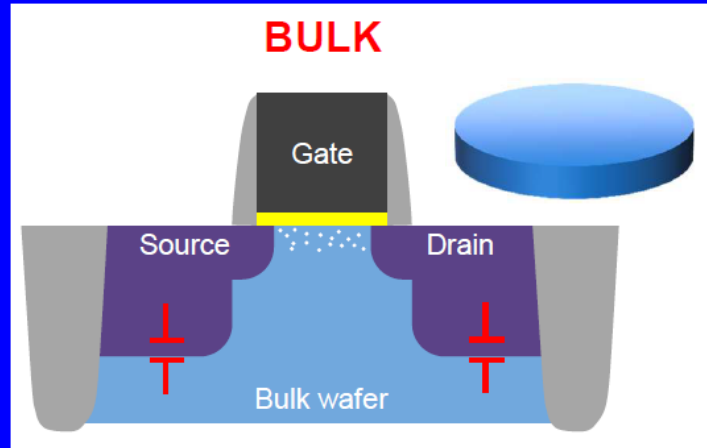
Sub-threshold slope:  $S = n \frac{kT}{q} \ln(10)$

Gain (strong inversion):  $\frac{g_m}{I_D} V_A = \sqrt{\frac{2 \mu C_{ox} W L}{n I_D}} V_A$



# FD-SOI Transistor Level Benefits

Source: GF 22FDX™ Platform



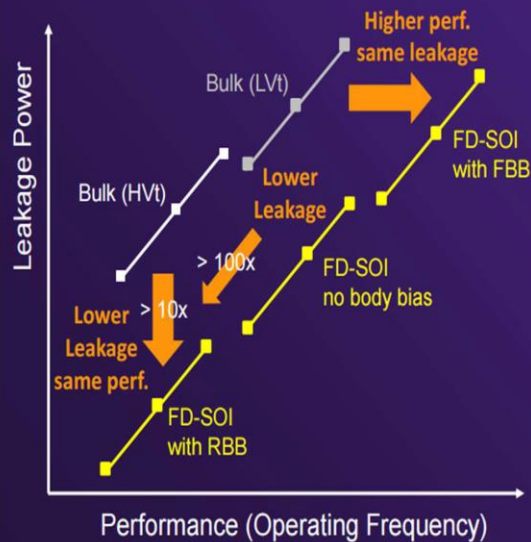
- $V_{th}$  and SCE defined by complex and heavily channel and halo doping techniques
- Large  $V_t$  mismatch due to random dopant fluctuation => limit  $V_{dd}$  scaling
- Strong sensitivity to short channel effect
- Large junction capacitance ( $C_j$ ), GIDL and Diode leakage
- Limited well bias capability

- Vertical transistor layout determined by FD-SOI engineered substrate and undoped channel
- Significant improved  $V_t$  mismatch due to minimize random dopant fluctuation => enable  $V_d$  scaling down to 0.4V or lower
- Excellent SCE
- Minimum  $C_j$ , GIDL & diode leakages Extensive back bias capability

# FD-SOI Performance

Source: GF 22FDX™ Platform

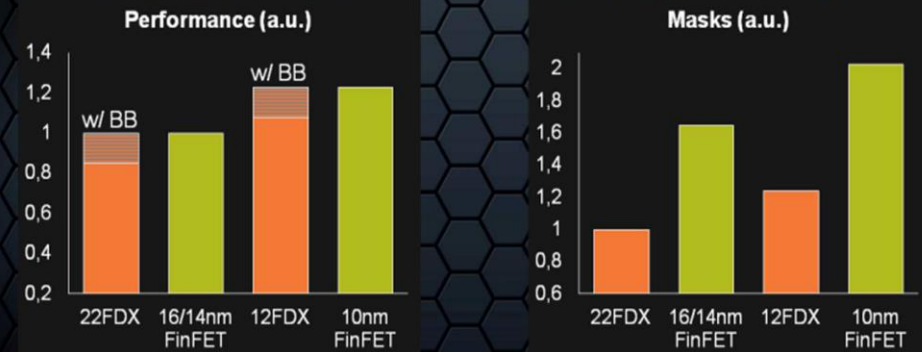
## FD-SOI Enabling Wide Dynamic Operating Range



- Outstanding Power-Perf demonstrated
  - Active mode @ 300MHz < 10mW
  - Deep-sleep with SRAM retained: < 2.5μW
  - Extremely low-leakage SRAM: ~ 0.5pA/bit
- Forward Body Bias (FBB) Expanded performance
- Reverse Body Bias (RBB) Lower leakage floor
- Dynamic biasing tunability

## FDX™ – The simple solution for advanced node performance

Next node performance with 40 percent fewer masks



FinFET digital performance & power  
Superior Analog/RF to FinFET  
Performance on demand w/ Body-bias

40% fewer masks  
Lower mask cost  
Reduced cycle time

Source: Based on GF internal assessments

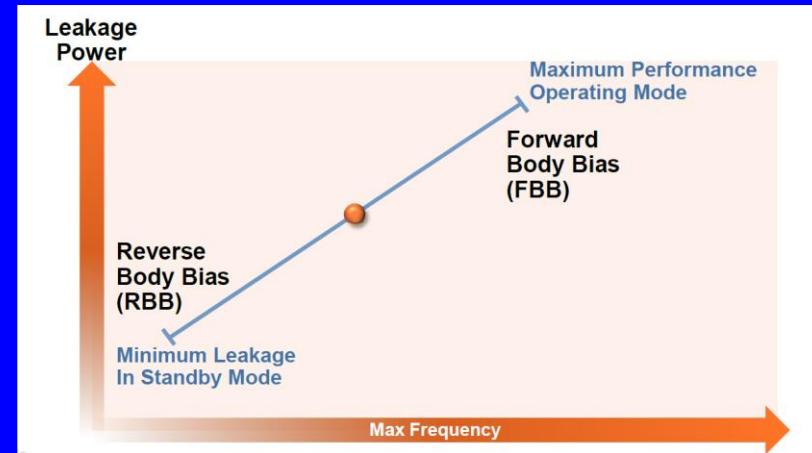
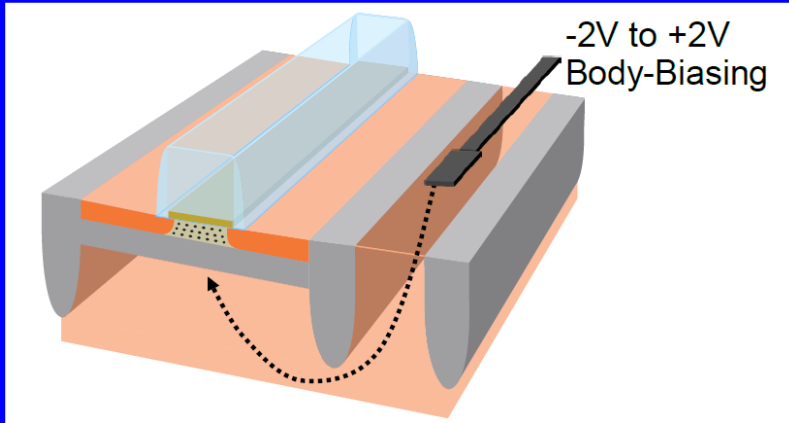
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Body-Bias enabling wider dynamic operating range

FD-SOI: FinFET performance at lower manufacturing cost

# FD-SOI enables “effective Body-Bias”

Source: GF 22FDX™ Platform



## Body-Bias provides greatest power efficiency and design flexibility

- Forward Body Bias (FBB) enables low voltage operation down to 0.4V
- Reverse Body Bias (RBB) enables low leakage down to 1pA/micron
- Dynamic body biasing enables active tradeoff of performance vs. power

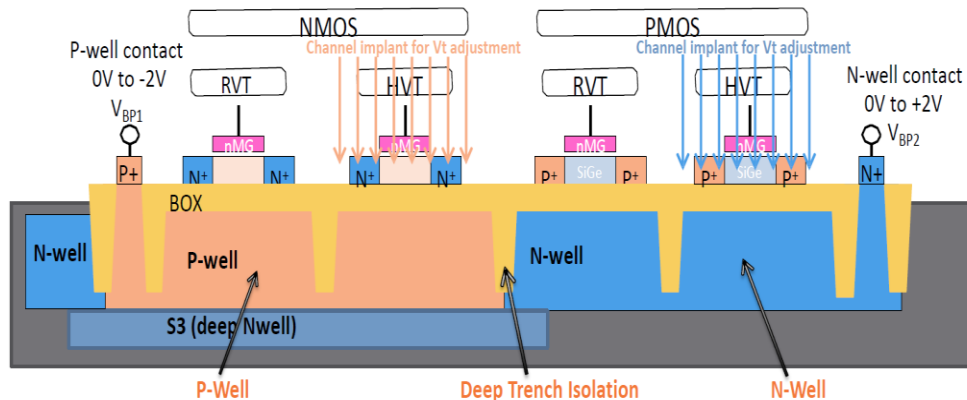
## Maximum Flexibility with Transistor Body Biasing

# Body Biasing Architecture

Source: GF 22FDX™ Platform

## Revers Body Biasing (RBB)

### 1.4 Body-Bias Architecture – RBB Technique in 22FDX (Conventional-well)



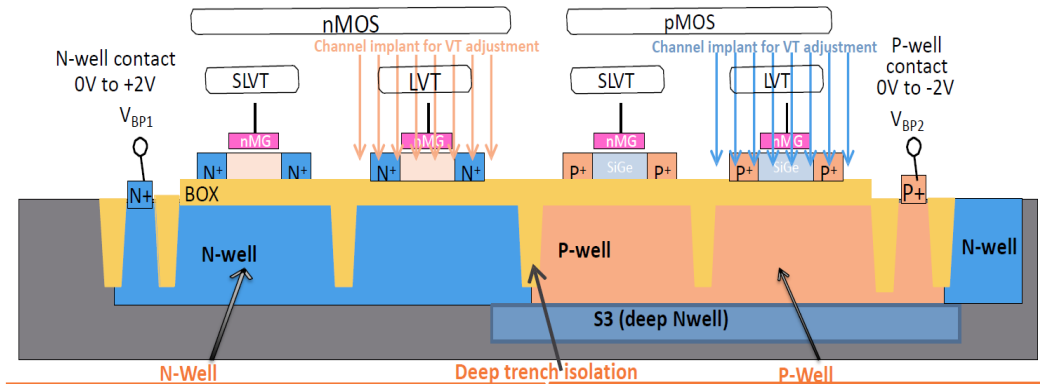
Within a P-well, the  $V_t$  regime of the transistor is changed by using a lightly p-doped channel implant

Within an N-well, the  $V_t$  regime of the transistor is changed by using a lightly n-doped channel implant

- There is a box between S/D and substrate and so:
  - No more parasitic diode between S/D & substrate
  - Only limitation is the parasitic diode between P-Well and N-Well and it will limit FBB operations
  - RBB can be run at much Higher voltage (current Models validated up to  $\pm 2V$  Bias)
  - Also, as channel is fully depleted body bias is more effective than in bulk technologies where the channel is heavily doped (70mV/V variation vs 25mV/V)
- RVT/HVT are swappable post PnR without area scaling impact
- Full RBB capability is possible with standard well scheme
- Gate length sizing for additional  $V_t$ /loff control

## Forward Body Biasing (FBB)

### 1.4 Body-Bias Architecture – FBB Technique in 22FDX (flip-well)

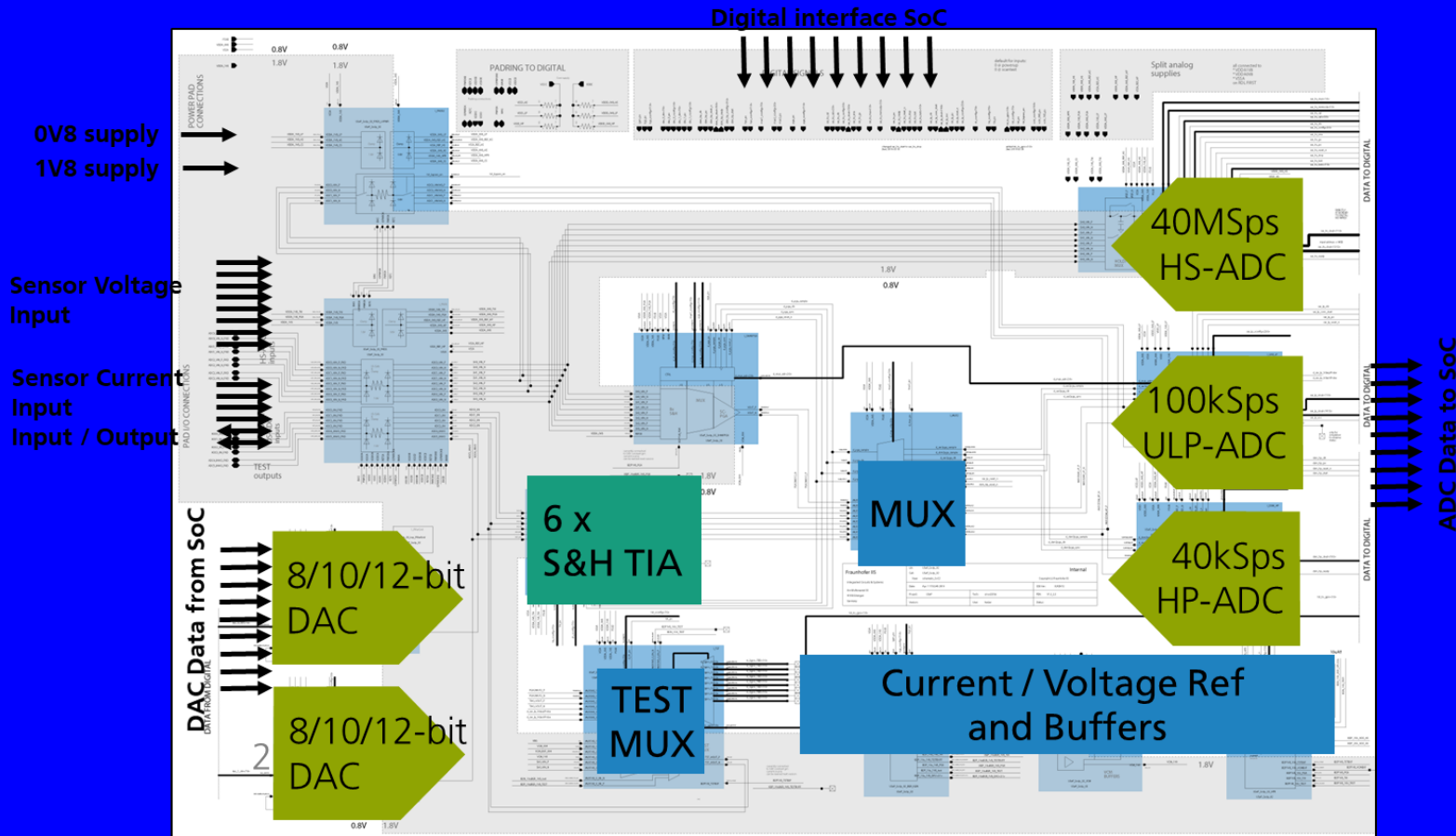


Within an N-WELL, the  $V_t$  regime of the transistor is changed by using a lightly p-doped channel implant

Within a P-WELL, the  $V_t$  regime of the transistor is changed by using lightly n-doped channel implant

- There is a box between S/D and substrate and so:
  - It is possible to enable the flip well architecture (NMOS on an NWELL, PMOS on a PWELL)
  - There is no more parasitic diode between S/D & substrate
  - Only limitation is the parasitic diode between P-Well and N-Well and it will limit RBB operations
  - FBB can be run at much higher voltage (current Models validated up to  $\pm 2V$  Bias)
  - Also, as channel is fully depleted body bias is more effective than in bulk technologies where the channel is heavily doped (70mV/V variation vs 25mV/V)
- SLVT/LVT are swappable post PnR without area scaling impact
- Full FBB capability is possible with flip-well scheme
- Gate length sizing for additional  $V_t$ /loff control

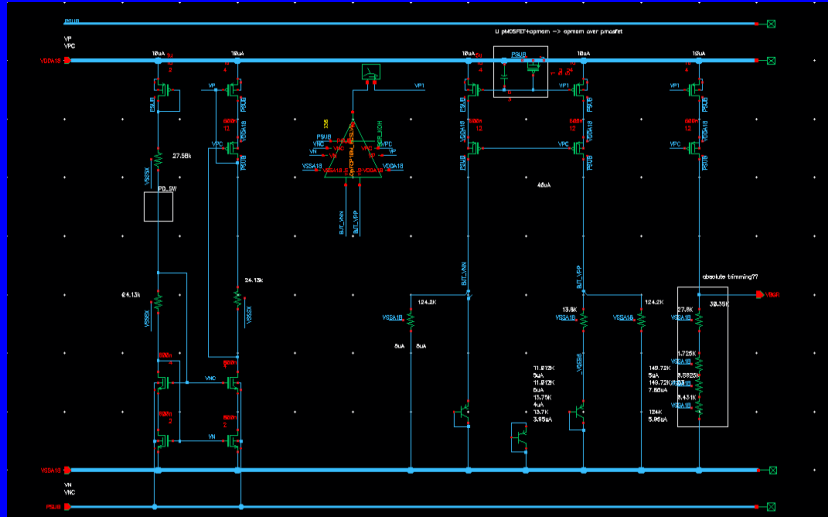
# Sensor Analog Frontends for IOT (22 nm FD-SOI)



Universal Sensing system for IOT application

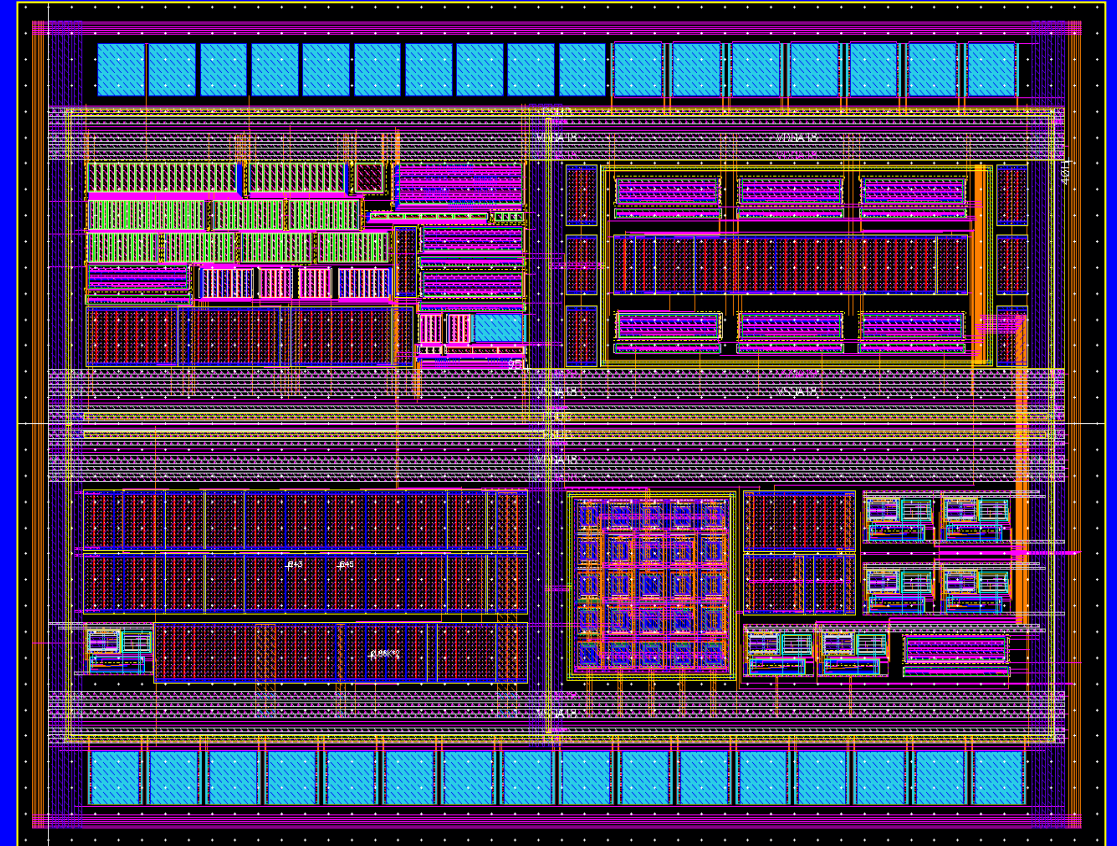
- The sensor technology integrated into the standard model already covers the acquisition of the majority of possible measurement parameters.
- This includes **bi- and triaxial acceleration, humidity, temperature, air pressure, gas, location and vibration.**
- GLOBALFOUNDRIES 22FDX<sup>®</sup> technology is chosen for low cost and high performance of the system.
- **22FDX is built according to the silicon-on-insulator principle (fully depleted SOI),** the highly integrated chip design permits the manufacture of particularly energy-efficient and cost-effective chips.

# Bandgap Reference in 22 nm FD-SOI

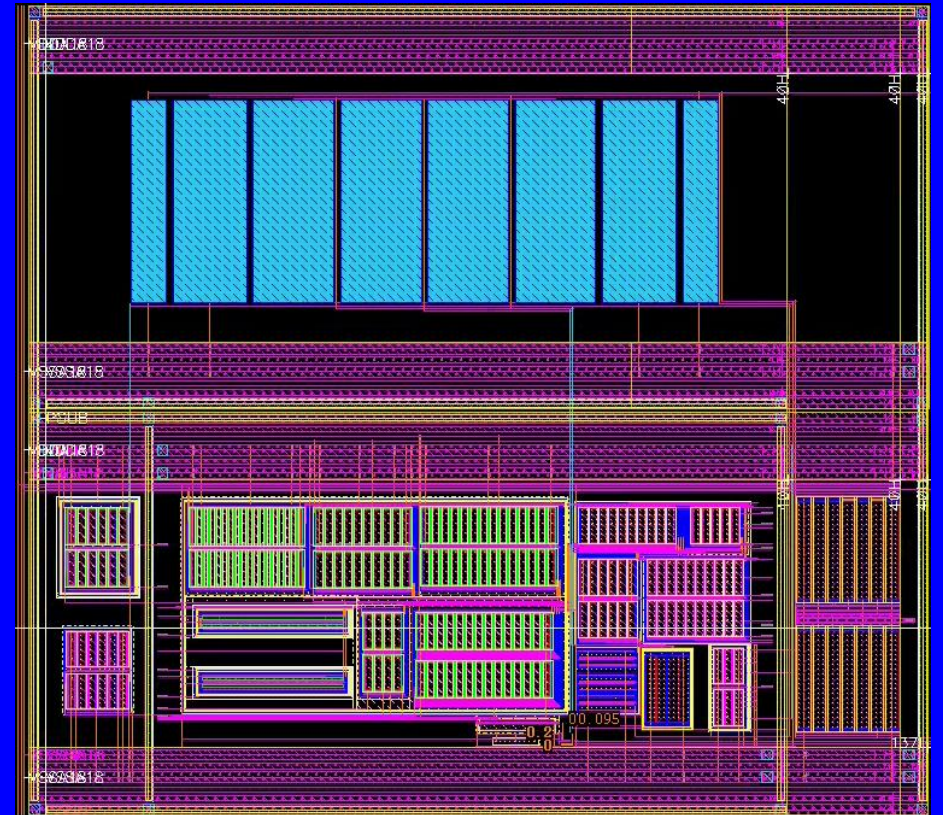
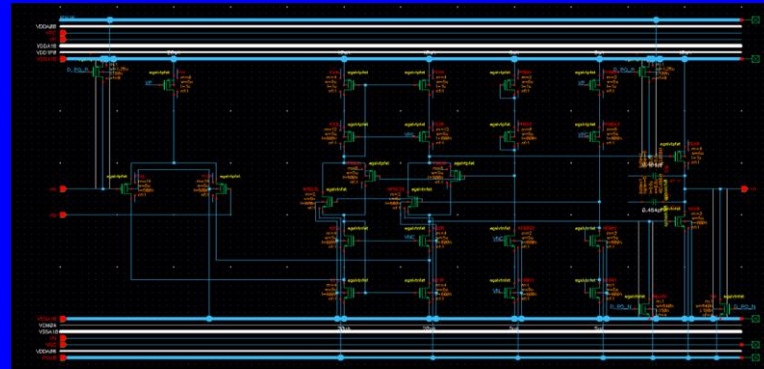
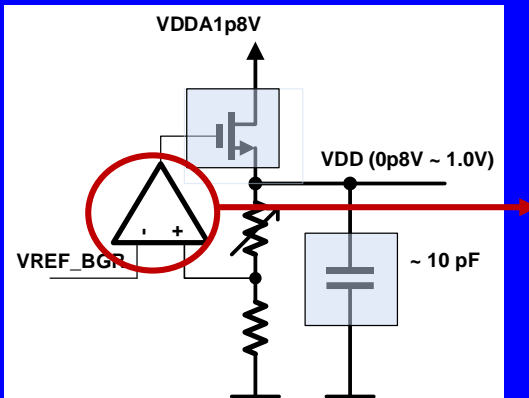


## BGR is presented here

- A sub 1.0 V current mode BGR (“Banba” BGR) is presented here for the low output voltage requirement
- $V_{DD} = 1.8V$ ,  $V_{OUT} = 0.4 V$
- Layout occupies an active area of  $215 \times 155 \mu m^2$



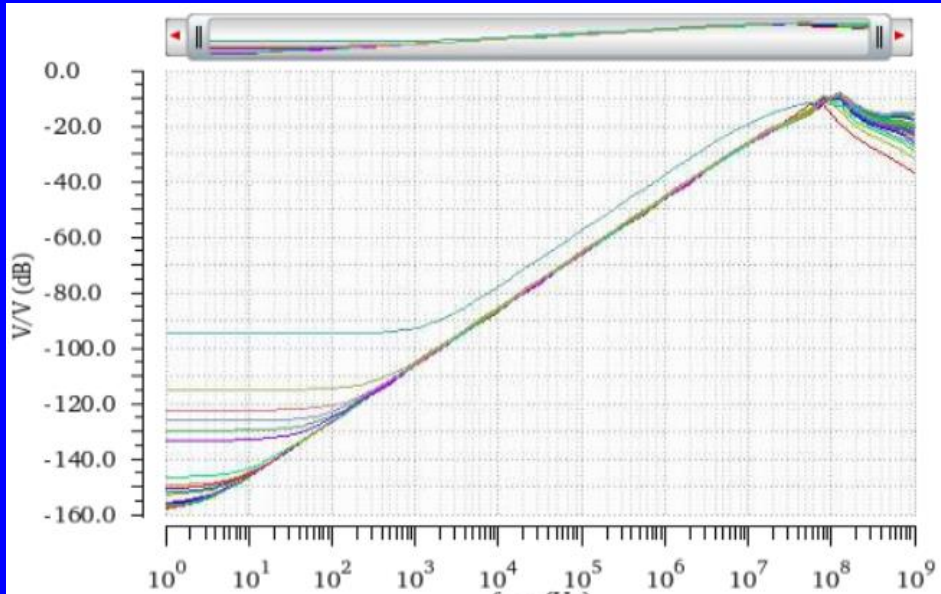
# “Capless” nMOS Regulator in 22 nm FD-SOI



## A capless nMOS Regulator is presented

- Class AB amplifier is adopted for better response of the Error Amp
- $V_{IN} = 1.8V$ ,  $V_{OUT} = 0.8V$
- No external compensation cap is needed.
- 10 pF is formed on silicon thanks to nMOS regulator pole location.
- Layout occupies an active area of  $140 \times 120 \mu m^2$

# “Capless” nMOS Regulator in 22 nm FD-SOI



## Design Result – Power Supply Rejection

- ILOAD= 0uA to 3mA
- Upto ILOAD=2.5mA ~60dB attenuation (1/1000) is maintained @200kHz

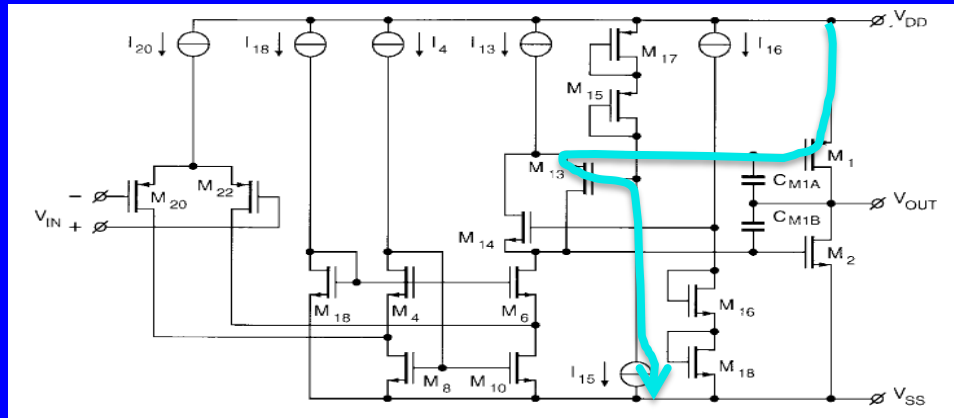
ITEM	MEASURE	ILOAD_Max
LDR	Vout(@ILOAD)=0.8V=VREF	3.1mA
LNR	LNR(@ILOAD) = 0.1%	1.3mA
PSR	PSR(@ILOAD) = 60dB@200kHz	2.5mA
STB	LOOPGAIN(@ILOAD) = 120dB, with PM=70'	1.8mA

## Trusted electronics

- nMOS Linear regulator supports ILOAD=1.3mA
- Required range ILOAD ~ 200uA or at best 300uA



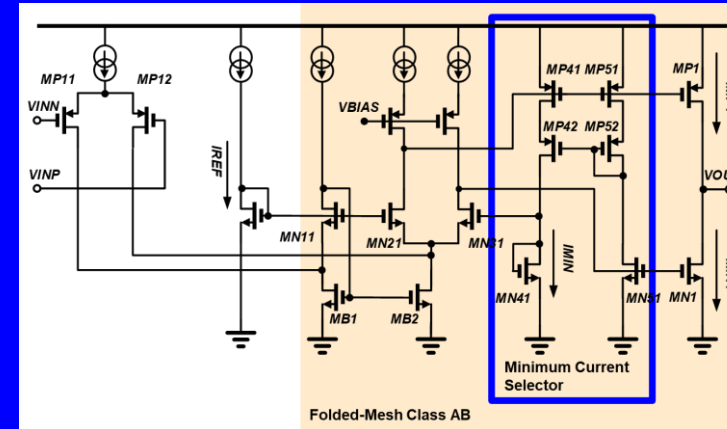
# Switched Capacitor PGA in 22 nm FD-SOI



R. Hogervorst et al, IEEE JSSC, Vol. 29, no. 12, 1994, pp. 1505–1513

**“Classic” Class AB Controller is not able to operate at 0.8 V VDD**

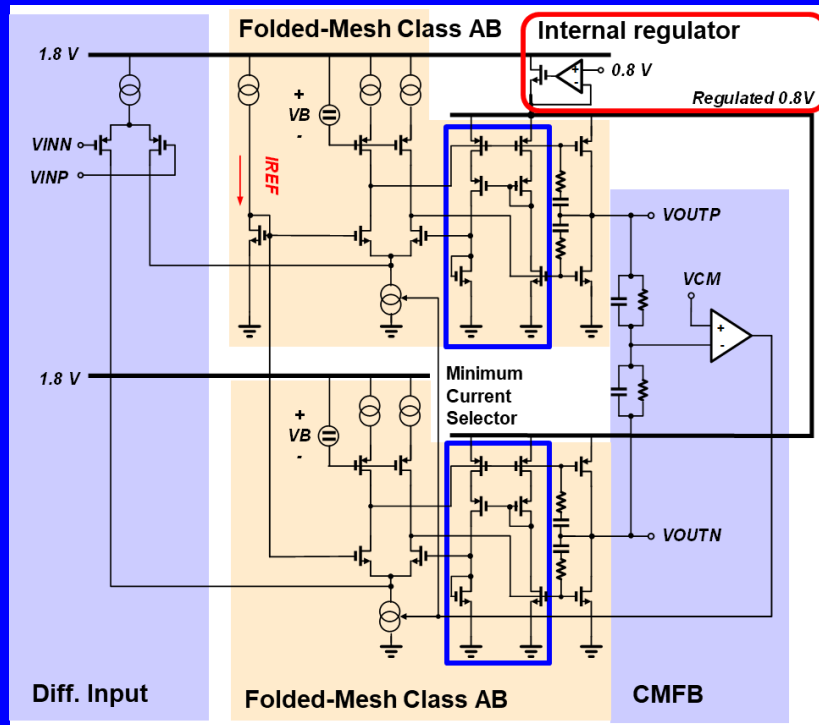
- Minimum power supply voltage is given as  $|VSGM1| + |VSGM13| + VDSAT115$
- VDD should be at least over 1.05 V for the correct operation
- **Class AB operation is guaranteed above 1.2 V VDD**



**We propose a two-stage folded-mesh with min. current selector for 0.8 V VDD operation**

- Minimum power supply voltage is given as  $|VSGMP1| + VDSATMN21 + VDSATMB2$
- VDD can be lowered to 0.65 V for the correct operation
- **Class AB operation is guaranteed at 0.8 V VDD in 22 nm FD-SOI process**

# Switched Capacitor PGA in 22 nm FD-SOI

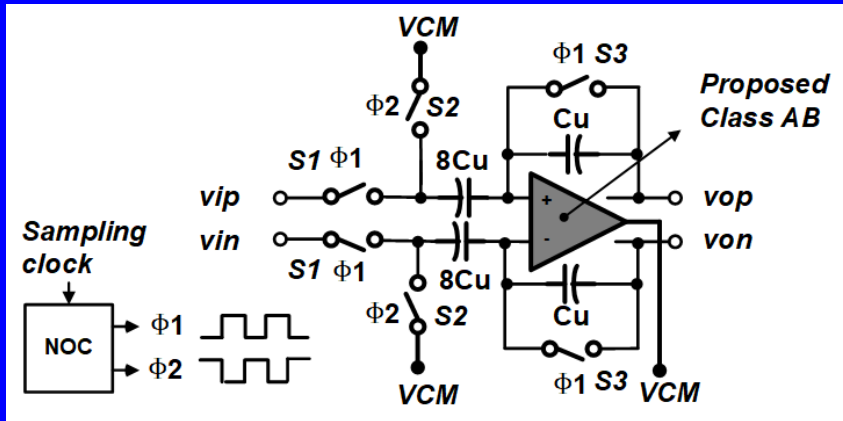


	Unit	TYP	MIN	MAX
Tech		22 nm FDSOI		
Supply	V	1.8	1.71	1.89
Area	mm <sup>2</sup>	0.0384 (0.32x0.12)		
Current Consumption	uA	387.7	386.4	390.6
Open-Loop DC Gain	dB	147.1	144.4	148.6
Open-Loop Unity Gain Bandwidth	MHz	58.9	17.6	40.8
Open-Loop Phase Margin	Degree	68.2	53.0	75.0
CM FB DC GAIN	dB	151.0	148.1	152.7
CM FB Unity Gain Bandwidth	MHz	54.3	18.5	44.9
CM FB Phase Margin	Degree	40.0	35.0	50.3
NM OSREG DC GAIN	dB	140.3	115.6	150.4
NM OSREG Unity Gain Bandwidth	MHz	35.4	25.7	61.6
NM OSREG Phase Margin	Degree	64.0	46.4	61.9
Slew Rate Low to High	V/usec	15.8	14.2	17.4
Slew Rate High to Low	V/usec	14.2	12.8	15.6

Now we extend this concept to a fully diff. op-amp

- The proposed class AB op amp implements successfully push-pull output current driving capability with 1.8 V input to 0.8 V output level-shifting, thanks to the internal regulator.

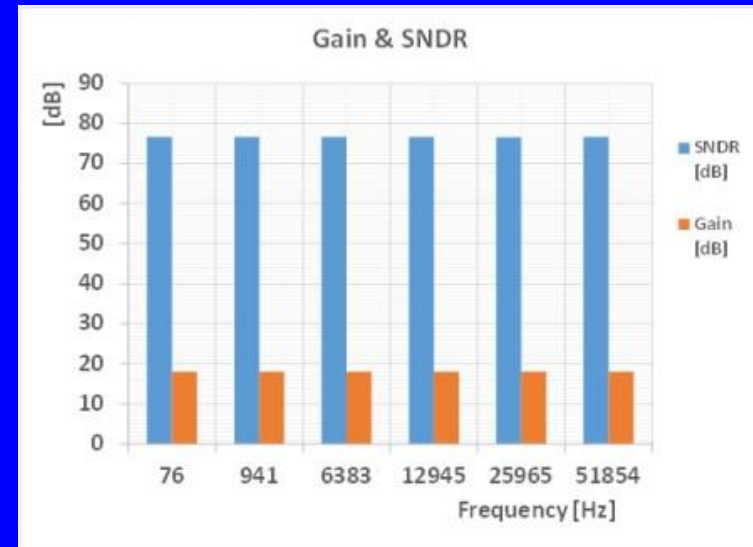
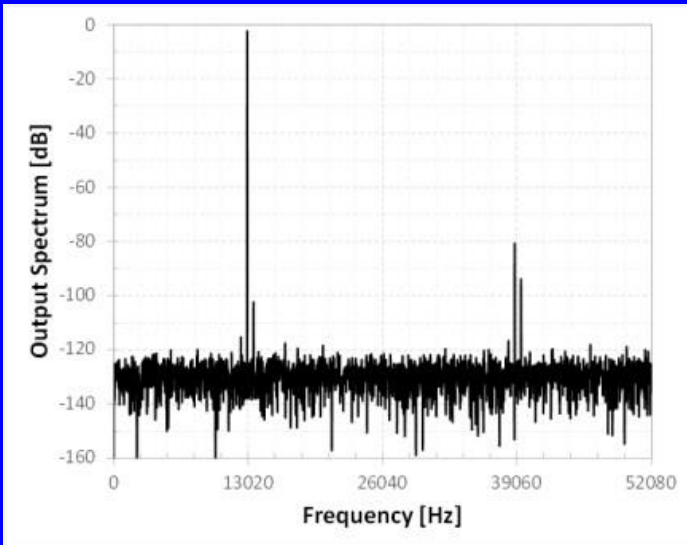
# Switched Capacitor PGA in 22 nm FD-SOI



**As a concept-demonstration, a switched capacitor amplifier with the proposed class AB is presented**

- Non-overlapping clocks  $\Phi1$  and  $\Phi2$  are generated internally with an external 104.2 kHz sampling clock
- 0.5 pF is chosen for the unit capacitor  $C_u$
- All implements are made in a 22 FD-SOI CMOS technology
- The switched capacitor amplifier occupies active area of 0.0946 mm<sup>2</sup>
- Area of proposed operational amplifier is 0.0384 mm<sup>2</sup>.

# Switched Capacitor PGA in 22 nm FD-SOI



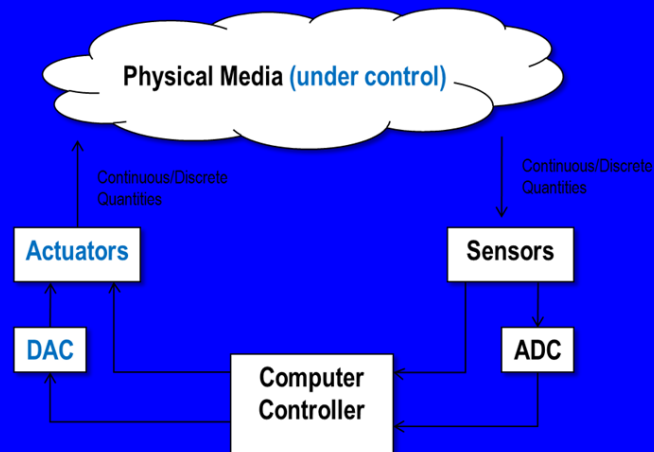
## Measurement Results

- 12.4 bit accuracy with 95 mV<sub>peak</sub> sinusoidal input with 12.945 kHz is sampled at a sampling frequency of 104.2 kHz
- 76.5 dB for SNDR and 77.3 dBc for SFDR are obtained
- 18 dB Gain are obtained from 76 Hz to 51.854 kHz in the same conditions

**A 1.8 V-to-0.8 V input/output signal swing limited fully differential folded-mesh class AB operational amplifier is developed**

- Low power supply folded mesh Class AB is presented.
- An internal regulator where “external” 1.8 V is regulated to 0.8V
- Output swing ranges are limited to 0.8 V
- No additional 1.8V-to-0.8V signal level shifter is needed.

# Current Steering DAC in 22 nm FD-SOI



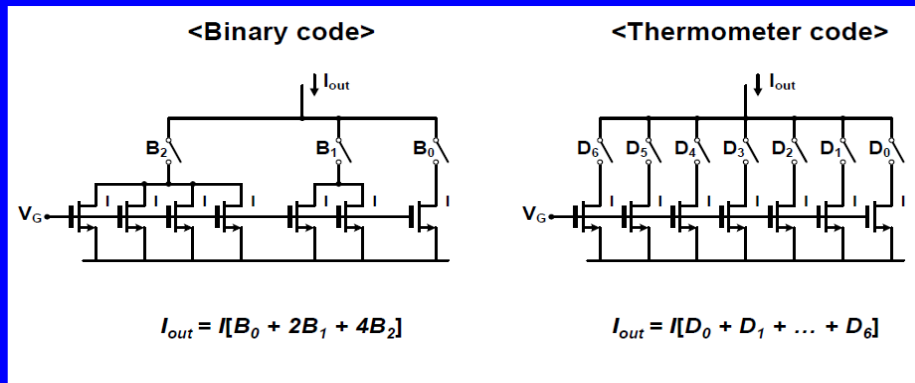
## DACs are used for a correction/calibration purpose

- Example : Closed-loop operation of Sensor-Actuator Systems in automotive, industrial and mobile device, where DAC is to drive an actuator
- Voltage offset, gain or current bias in an actuator require some timely adjustments or corrections for performance enhancement of a sensor read out circuit

## When a resistive actuator (load) needs to be driven in sensor-actuator systems, the DAC is required to have good output current driving capability

- Mostly, sensor-actuator system does not require a high speed, high accurate and high linearity of the DAC of the system [6]
- CS-DAC is the most suitable architecture for this case, since it naturally provides current as an output variable
- Some sensor-actuator systems pose a challenge
- Maximum output current needs to be correspondingly varied with a configurable resolution
- Motivation
- CS-DAC is required to have a resolution programmability for maximum output current driving capability

# Current Steering DAC in 22 nm FD-SOI



	Binary-Weighted	Unary Weighted
Decoder	No need, simple	Need, complex
Glitch	Huge (transition 011...1 to 1...000)	Less
DNL	Bad	Good

## Binary-Weighted Architecture and Unary-Weighted Architecture are popularly used for implementation of CS-DAC

- Both has PROS and CON

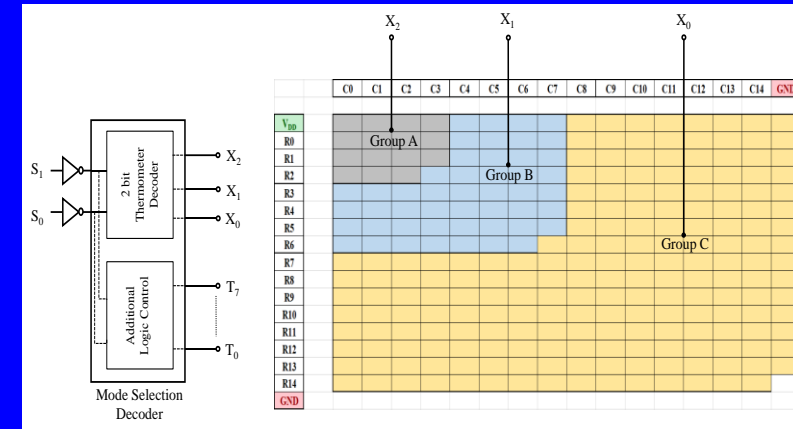
### Application to CS-DAC Architecture

- MSBs (Most Significant Bits) conversion → UW architecture
- LSBs (Least Significant Bits) conversion → BW architecture

Now question arises how to make a good segmentations !

# Current Steering DAC in 22 nm FD-SOI

Resolution	Unary Weighted	Binary-Weighted	Segmentation Level [%]
8	4	4	50.0
10	6	4	60.0
12	8	4	66.7



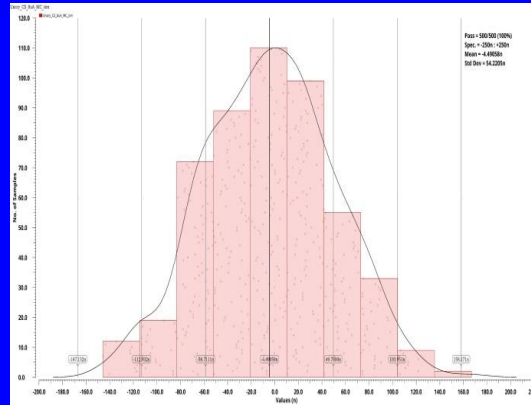
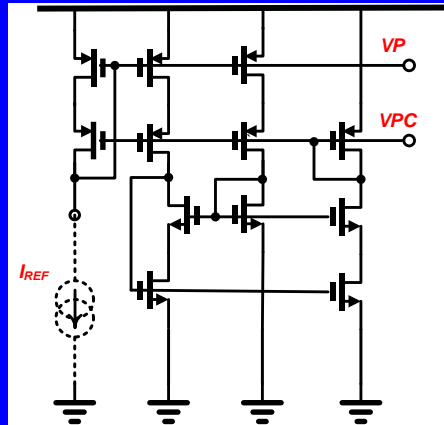
We propose “optimized segmentation” level of the “resolution programmable” CS-DAC based on “Area Optimization Method”

- CS-DAC is designed to have **DNL of 0.5 LSB** and **INL of 1 LSB** at three different resolution modes

We propose “Grouping-Selection” of the necessary unary cells in the 2-D unary matrix

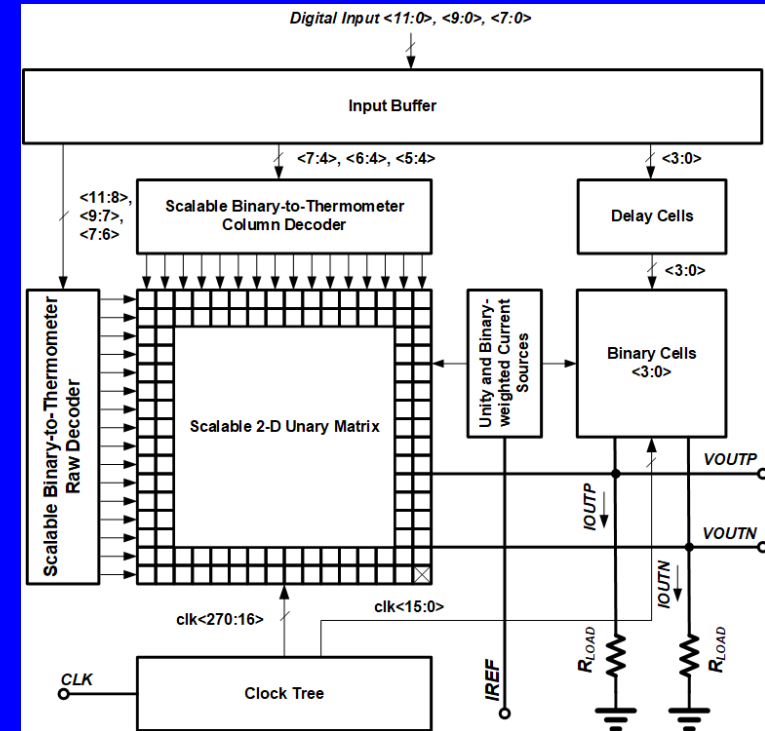
- Resolution programmability is achieved by proposed „Grouping-selection” using a “resolution mode selector”

# Current Steering DAC in 22 nm FD-SOI



In segmented CS-DACs,  $INL \propto$  Unary Current Source Variations

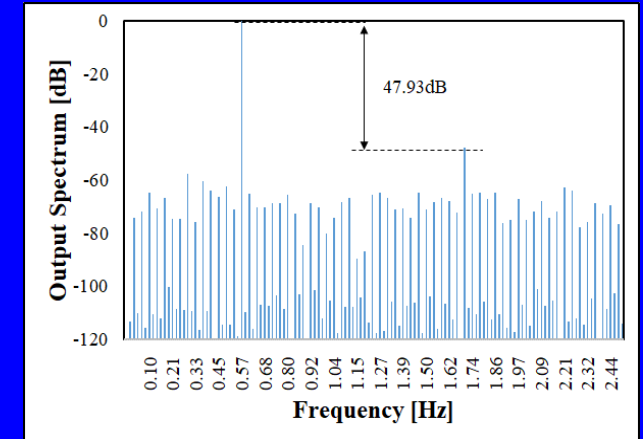
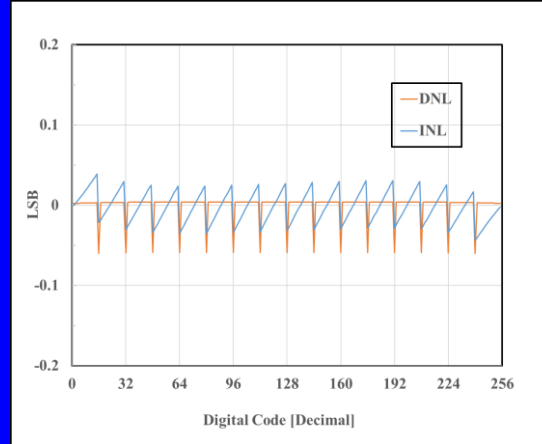
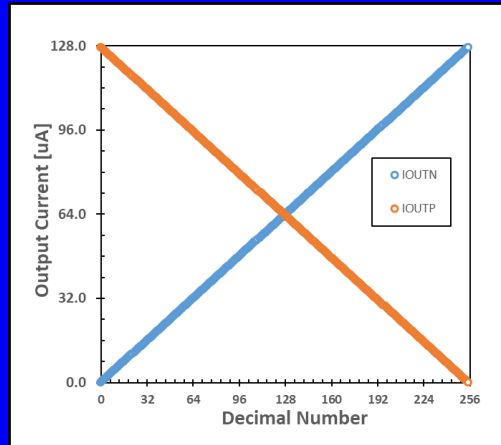
- Mismatch-aware design method was used
- The method was verified for current source using Monte-Carlo Simulation (with a specification range of  $\pm 0.5$  LSB)



Now we present the completed resolution programmable CS-DAC



# Current Steering DAC in 22 nm FD-SOI



## Full Current Driving Capability (resolution programmability)

- 250  $\Omega$  RLOAD is terminated here

## 8 bit-mode CS-DAC – Static and Dynamic Performances

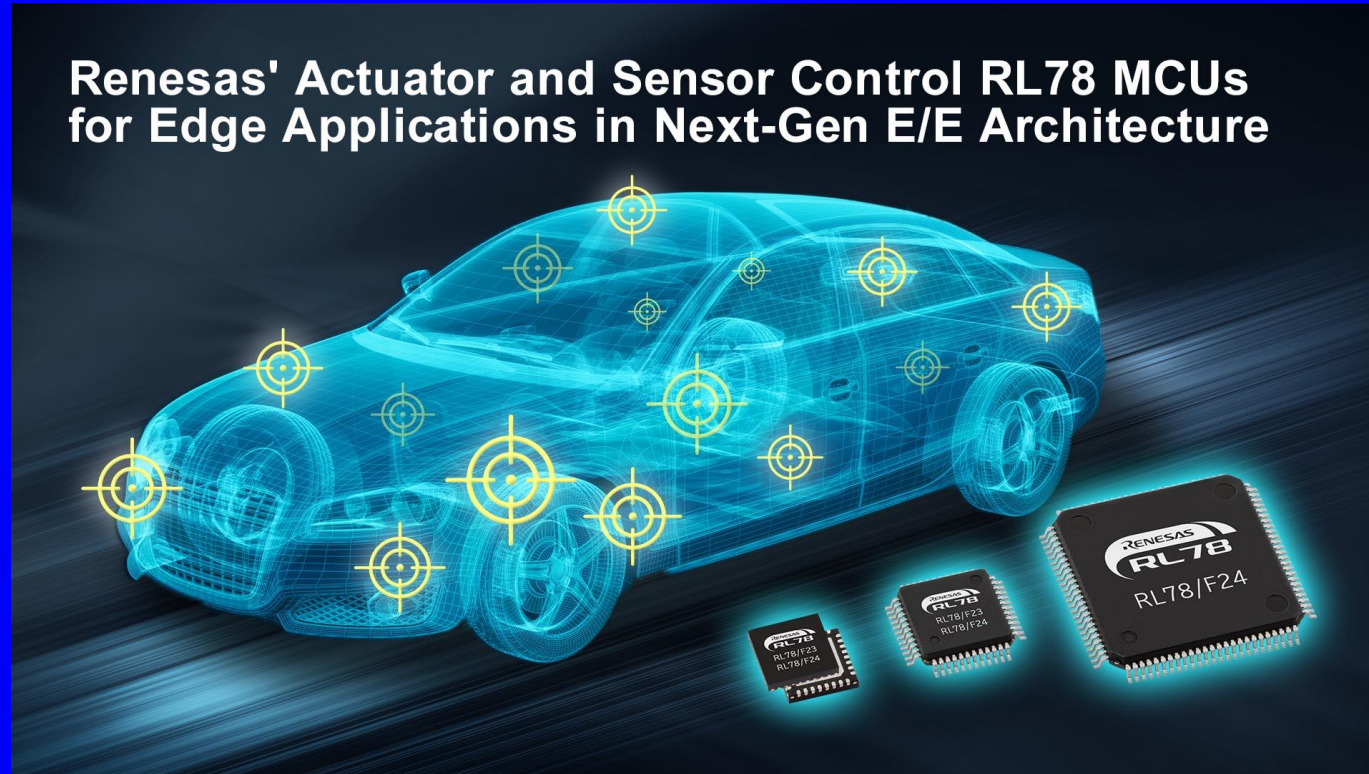
- Static Performance : DNL of 0.06 LSB and INL of 0.04 LSB are obtained
- Dynamic Performance : 47.93 dBc is obtained for SFDR

Resolution [bit]	8	10	12
Segmentation [U:B]	4:4	6:4	8:4
Supply [V]	0.8		
Rate [MS/s]	5		
DNL [LSB]	0.06	0.04	0.08
INL [LSB]	0.04	0.06	0.53
SFDR [dBc]	47.9	73.9	52.4
Power [mW]	0.214	0.513	2.407

# Renesas Electronics

- Automotive IC

Renesas' Actuator and Sensor Control RL78 MCUs for Edge Applications in Next-Gen E/E Architecture



- Low supply current to reduce power consumption (critical for hybrid vehicles)
- Excellent electromagnetic compatibility and ESD protection
- Stable performance at wide operational temperature range (-40 °C to +150 °C)
- Meet Functional Safety Requirement (ISO 26262)

# Renesas Electronics

- Focus Segment



**Automotive**

Highly reliable vehicle control, safe & secure autonomous driving and eco-friendly electric vehicles



**Industrial**

Lean, flexible and smart industry



**Infrastructure**

Robust infrastructure, enabling safety and efficiency



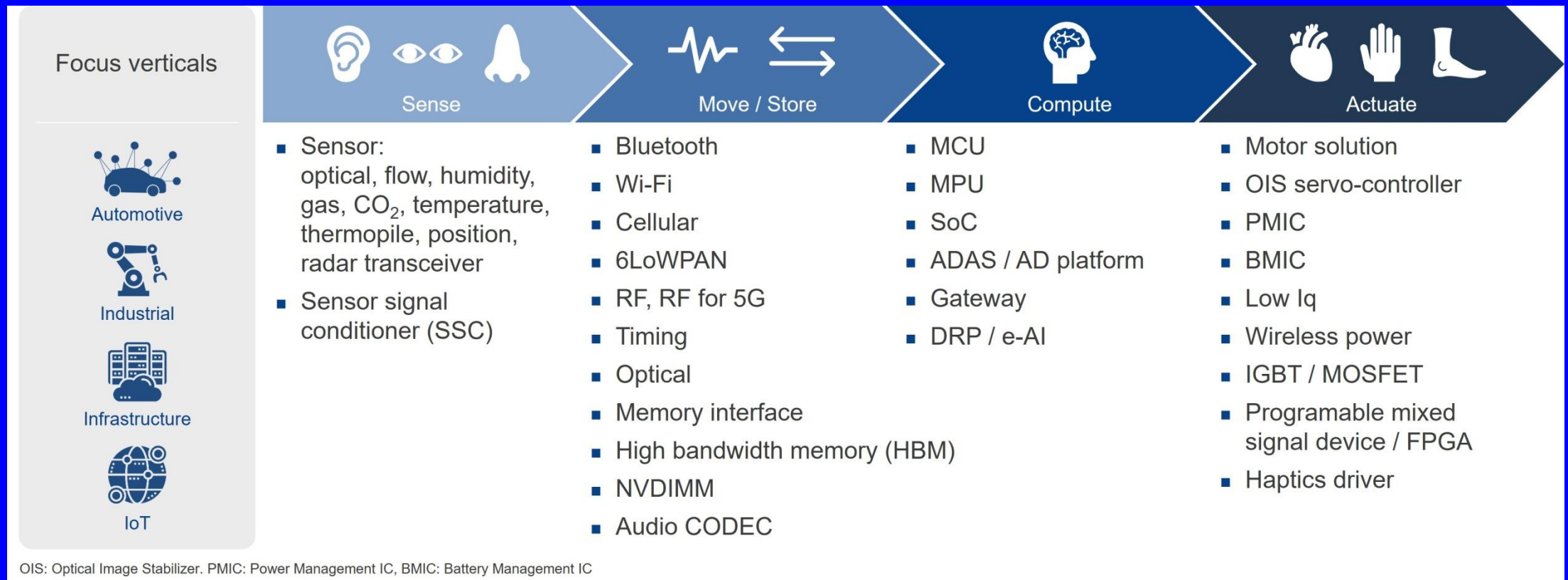
**IoT**

Comfortable, safe and healthy lifestyles through IoT

- **Renesas Electronics Corporation** is to develop a safer, healthier, greener, and smarter world by providing intelligence to our four focus growth segments: **Automotive**, **Industrial**, **Infrastructure**, and **IoT** that are all vital to our daily lives, meaning our products and solutions are embedded everywhere.

# Renesas Electronics

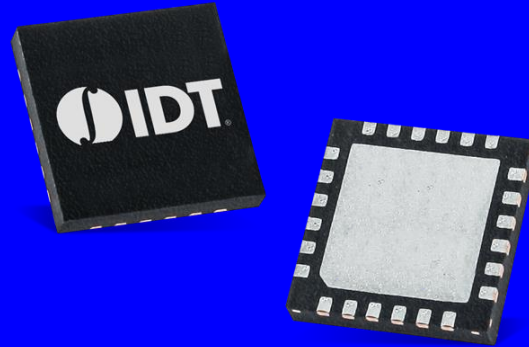
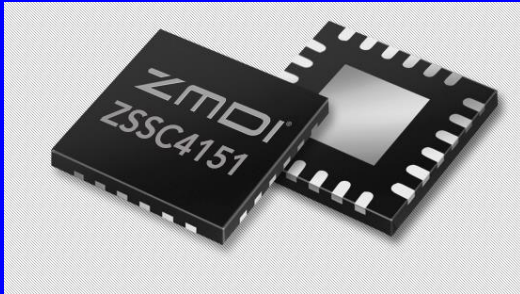
## • Product Portfolio



- **Renesas Electronics Corporation** designs and manufactures **microcontrollers, microprocessors, analog, power, and SoC products** for a broad range of **Automotive, Industrial, Infrastructure, and IoT applications**.

# Renesas Electronics

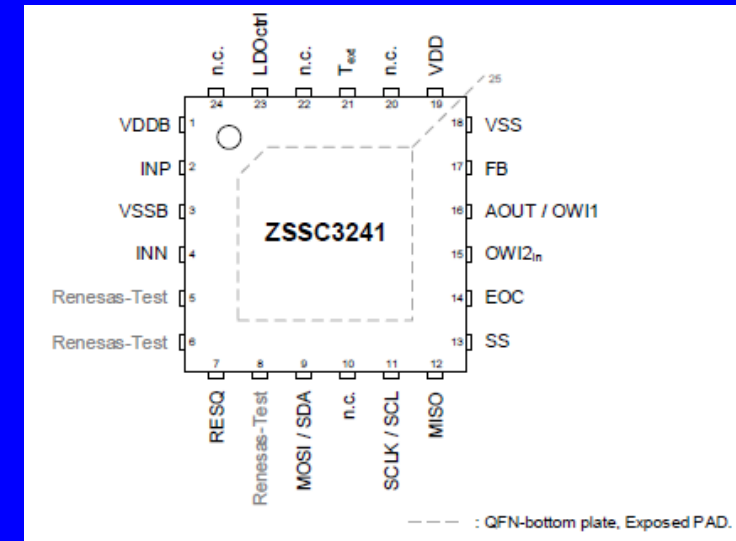
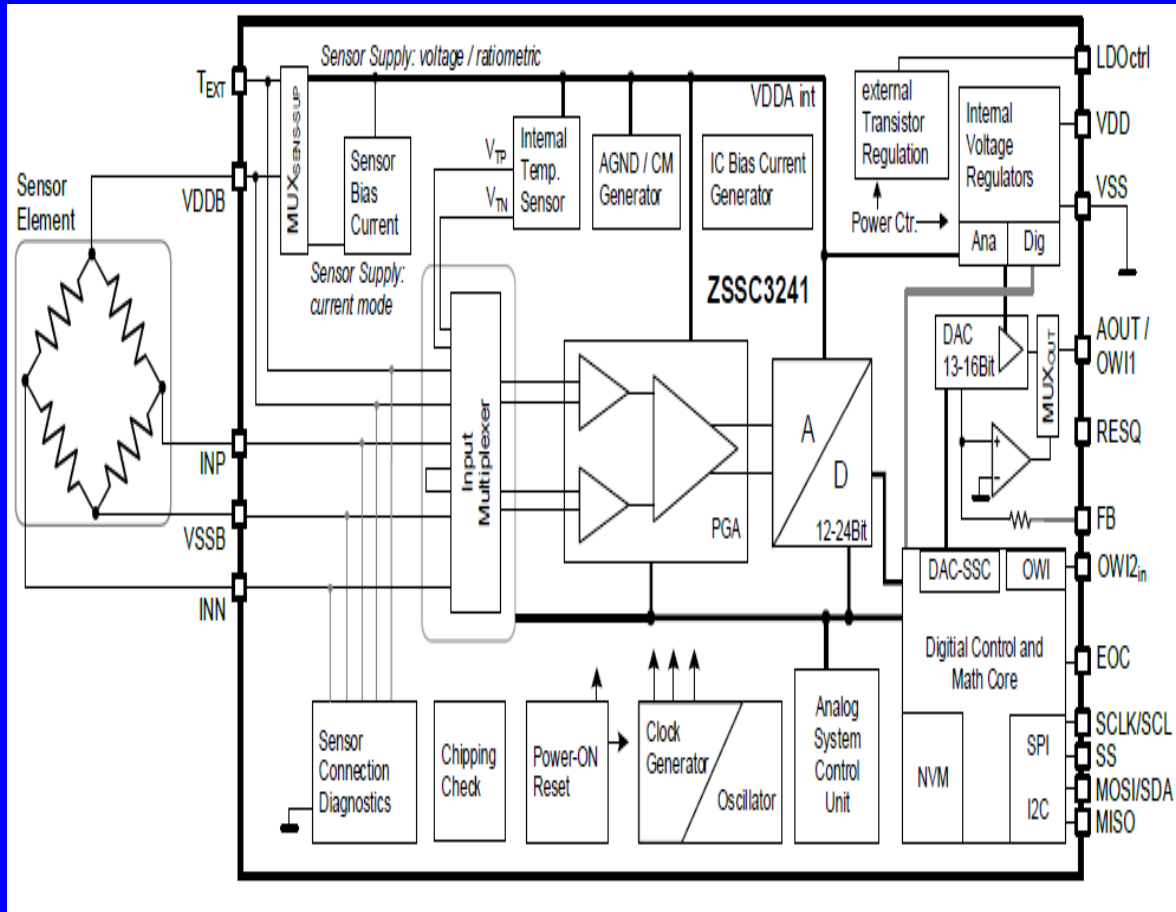
- Renesas Electronics Germany GmbH



- **Renesas Electronics Germany GmbH** is a leading provider of innovative, high-precision, robust and cost-effective **analog and mixed-signal ICs** for **automotive, industrial automation and consumer applications**.
- Renesas Electronics Germany GmbH (Formerly ZMDi AG) has been based in Dresden for over 50 years and is present worldwide. Since April 2019, the company has been part of Renesas Electronics Corporation with around 22,000 employees worldwide.

# CMOS Sensor Analog IP's Products

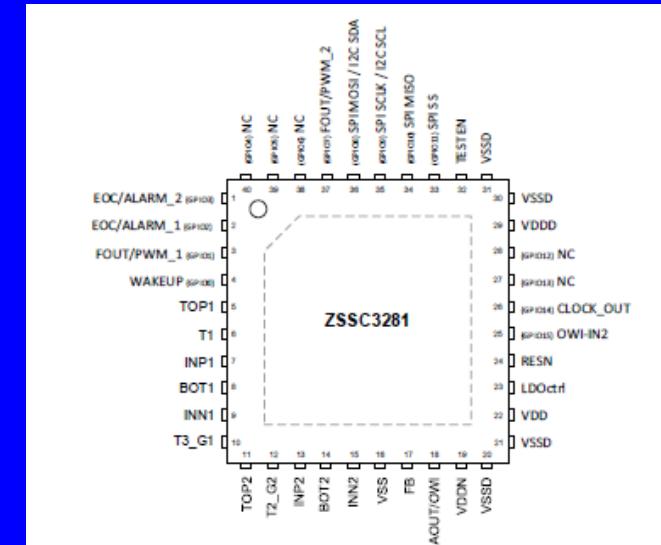
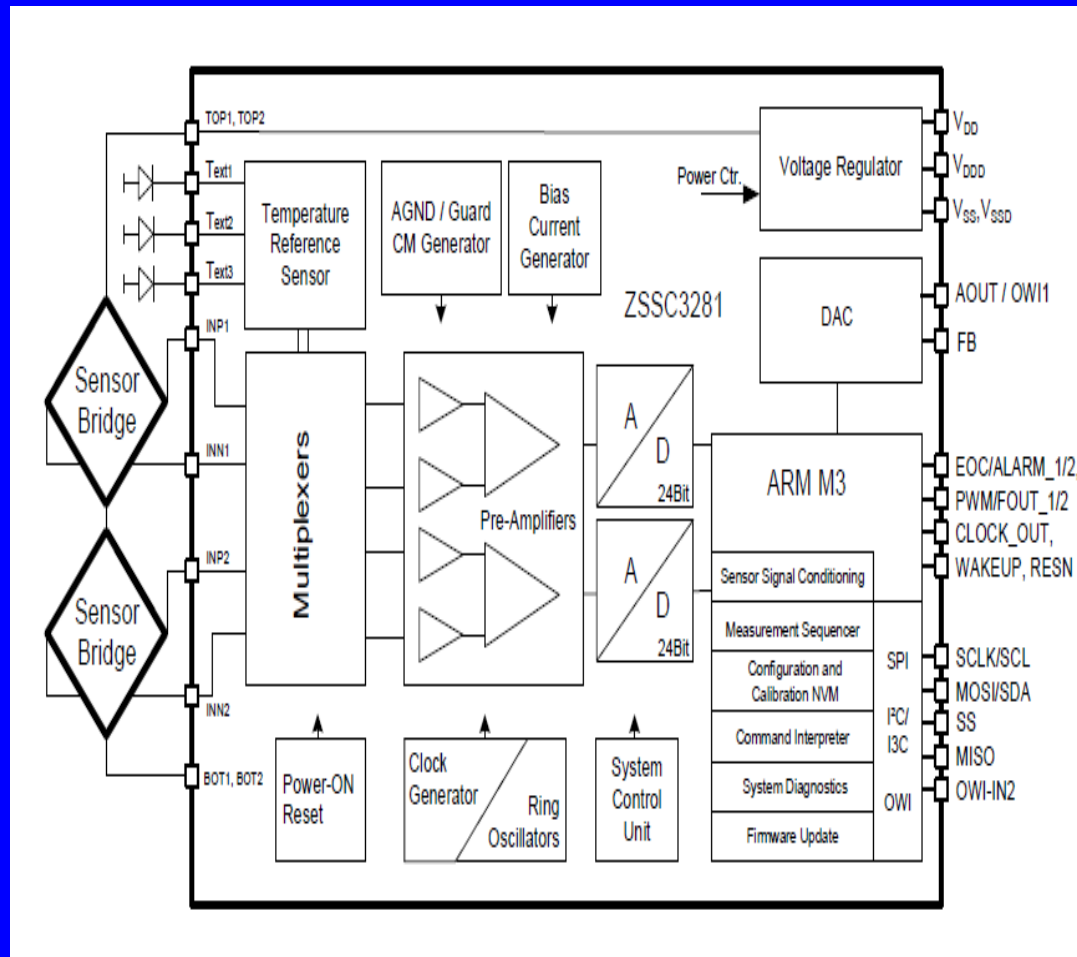
- ZSSC3241



- Physical Supply voltage, VDD: 2.7 V to 5.5 V
- Operating temperature: -40 °C to 150 °C
- Supported sensor elements: 0.5 kΩ to 60 kΩ
- ZSSC3241 is available in a 24-QFN package, (4x4 mm<sup>2</sup>)

# CMOS Sensor Analog IP's Products

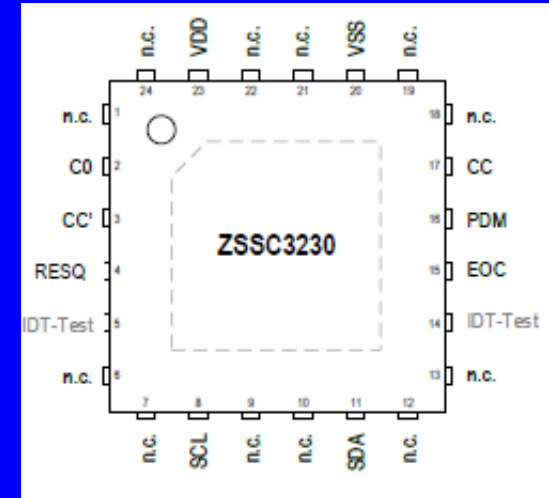
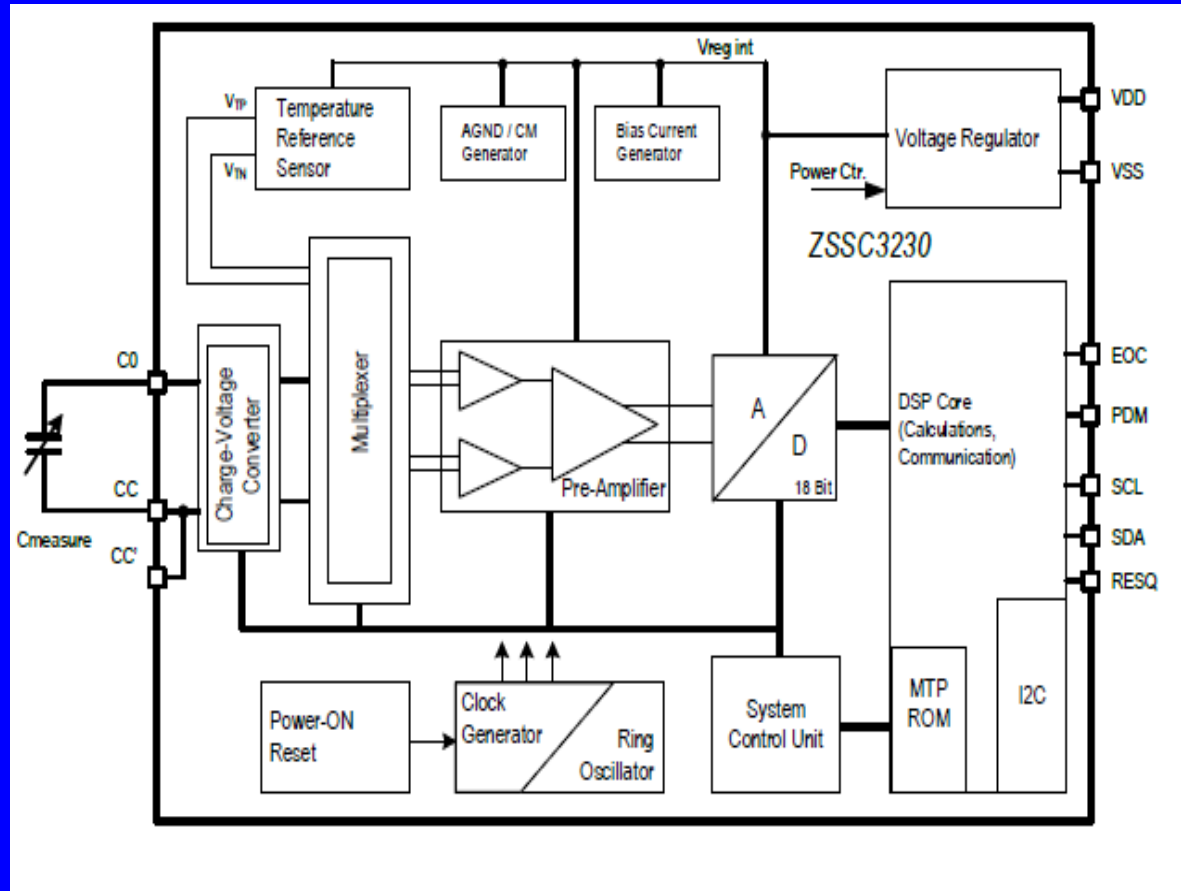
- ZSSC3201



- Physical Supply voltage, VDD: 1.8 V to 5.5 V
- Operating temperature: -40 °C to 150 °C
- Supported sensor elements: 0.825 kΩ to 60 kΩ
- ZSSC3281 is available in 40-QFN (5x5 mm<sup>2</sup>)

# CMOS Sensor Analog IP's Products

- ZSSC3201



- Physical Supply voltage, VDD: 1.68 V to 3.6 V
- Operating temperature: -40 °C to 150 °C
- Supported sensor elements: 0 pF to 30 pF
- ZSSC3281 is available in 24-QFN package, (4x4 mm<sup>2</sup>)



**Many thanks for your attention !!**

**DR.-ING. JEONGWOOK KOH**

Principal Analog Engineer  
Sensor Solution Department  
IoT and Infrastructure Business Unit

**Renesas Electronics Germany GmbH**

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