KIAT 한국산업기술진흥원
Korea Institute for Advancement of Technology

저전력 지능형 반도체 소자를 위한 물질 및 기술

2023년 7월 26일

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University of Nevada, Reno, NV 89557, USA
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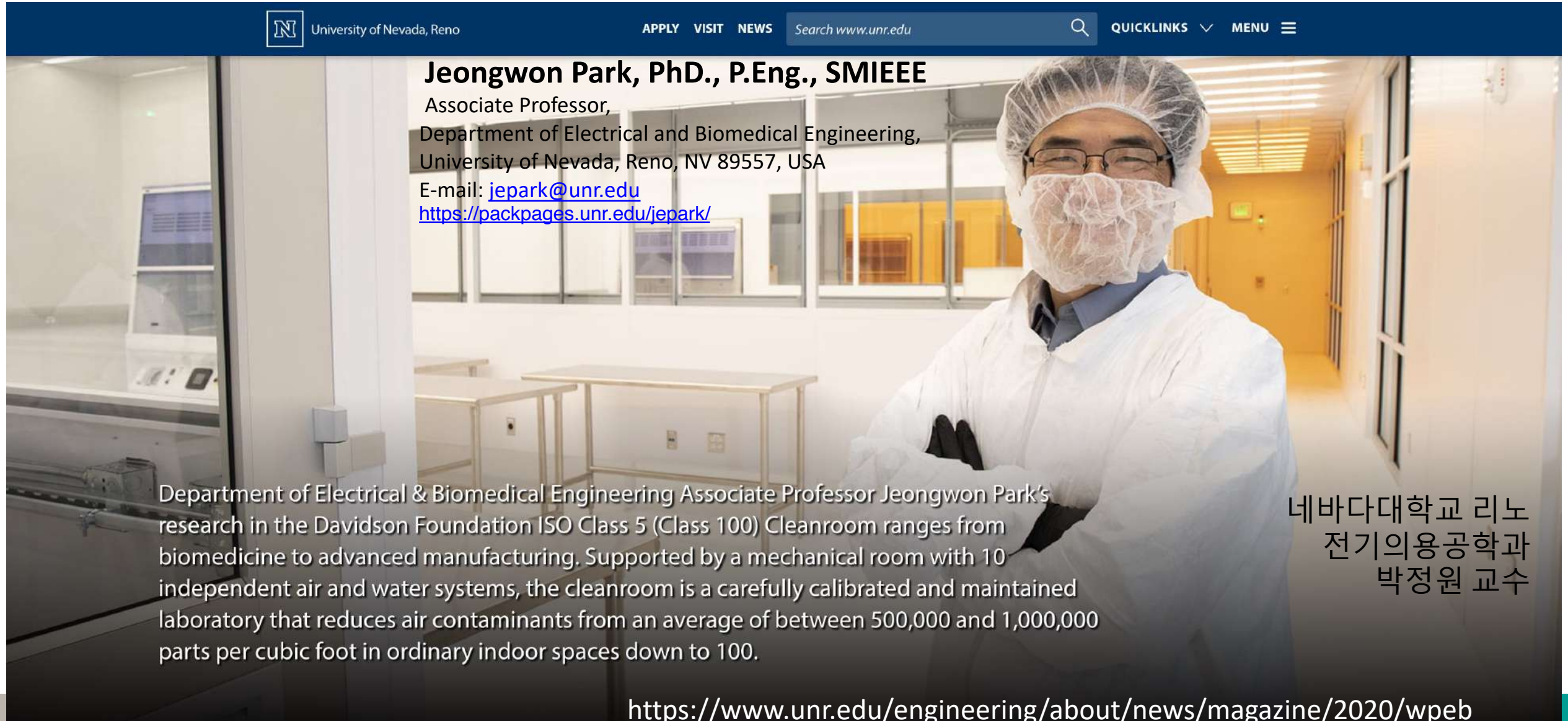
https://packpages.unr.edu/jepark/



네바다대학교 리노
전기의용공학과
박정원 교수

https://www.unr.edu/engineering/about/news/magazine/2020/wpeb

Semiconductor Materials and Devices for Low-power Artificial Intelligent Semiconductor Chips

Jeongwon Park, PhD.
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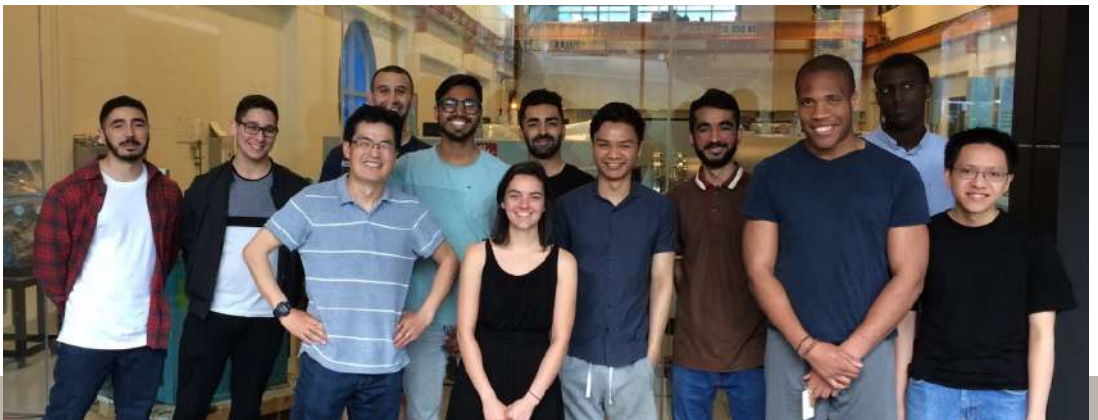
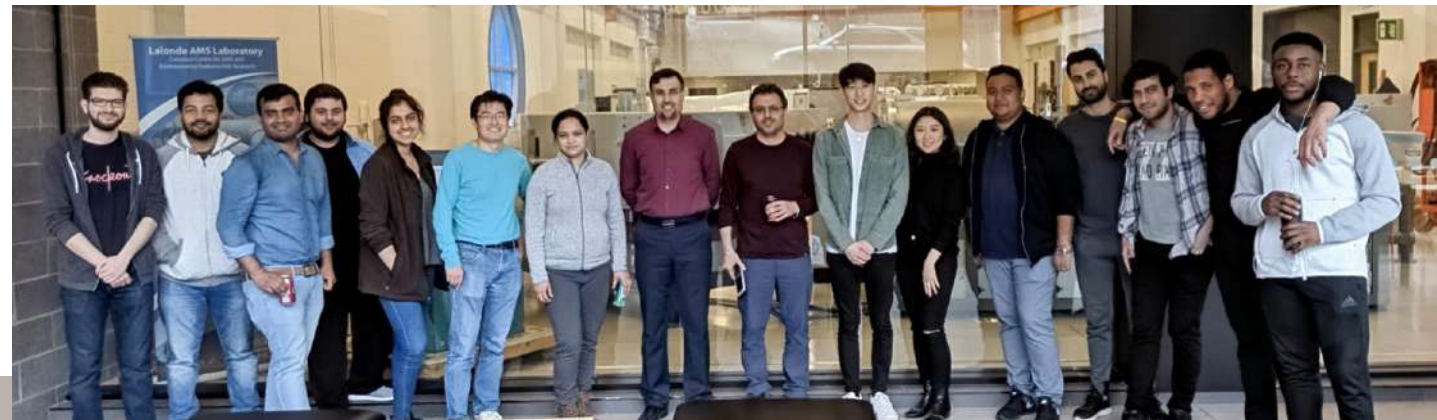


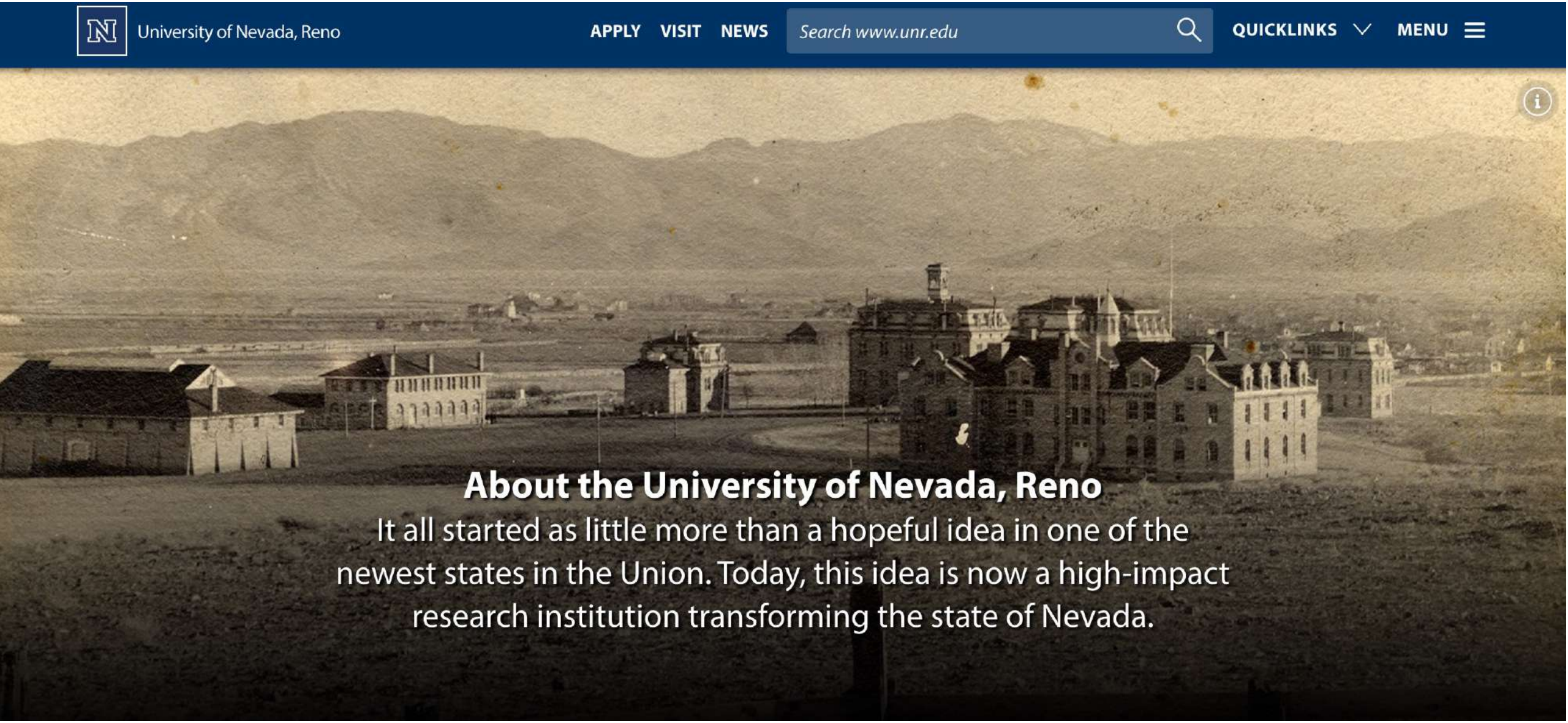



Medford
Redding
NEVADA
Reno
Sacramento
Yosemite National Park
Go-to destination for
outdoor activities
San Francisco
San Jose
Fresno
CALIFORNIA
Death Valley
National Park
Las Vegas
Bakersfield
Los Angeles
Anaheim
Long Beach
San Diego
Mexicali
Tijuana
Google
Satellite


Lake Tahoe

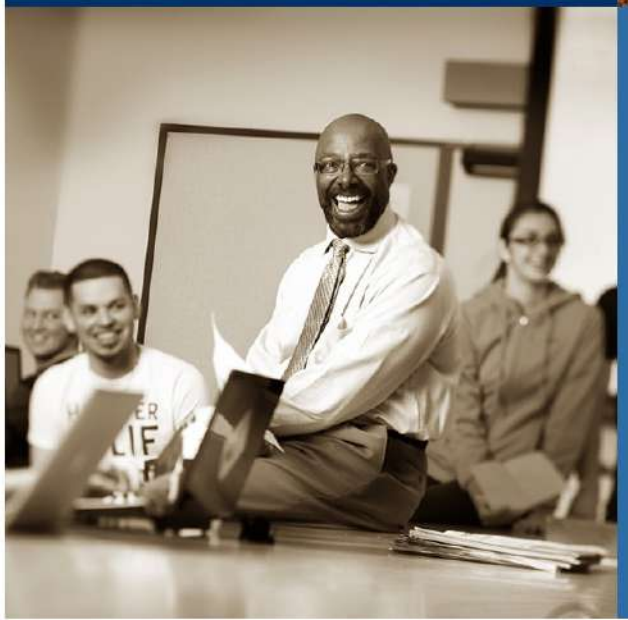

Yosemite national park

About the University of Nevada, Reno (UNR)

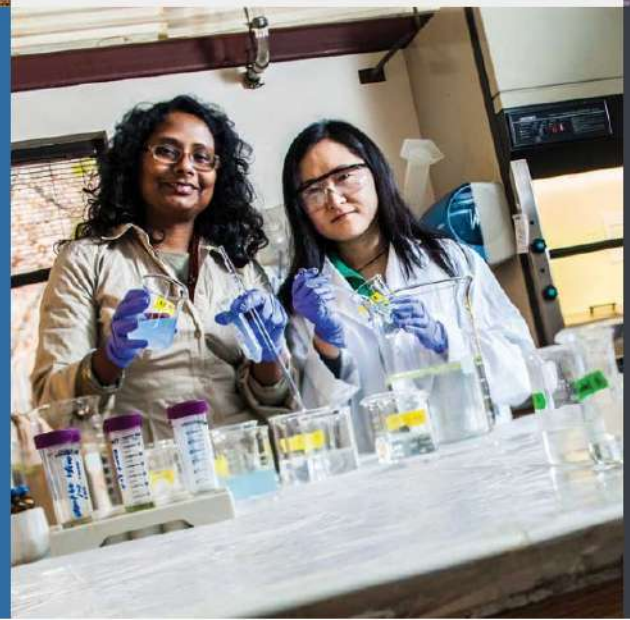


Founded in 1874

21,000+ students

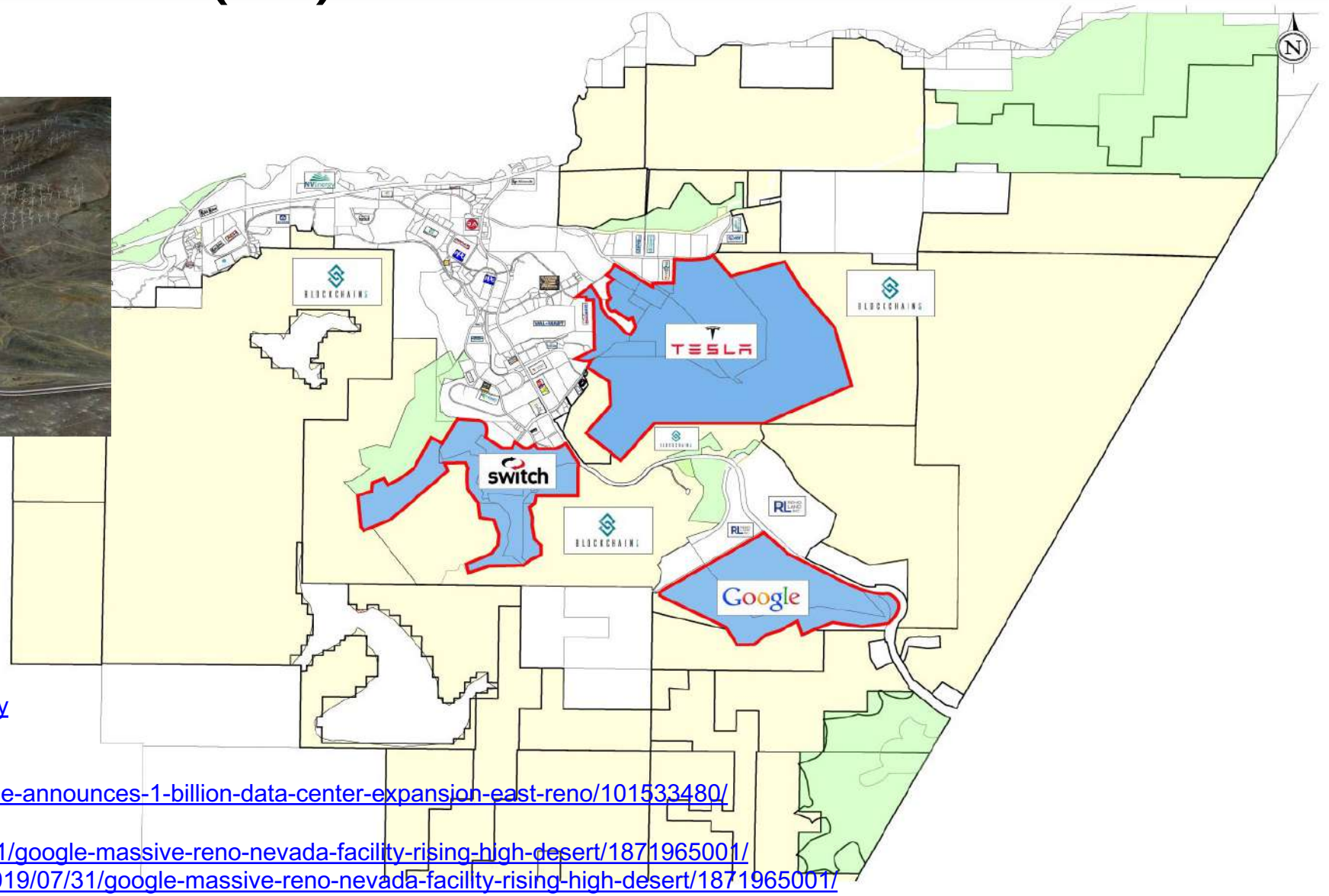


1,049 academic faculty



19:1 student-to-faculty ratio

Tahoe Reno Industrial Center (TRI)



- TESLA Gigafactory: https://www.tesla.com/gigafactory
- Apple data center:
- https://www.datacenters.com/apple-inc-reno
- https://www.usatoday.com/story/tech/2017/05/10/apple-announces-1-billion-data-center-expansion-east-reno/101533480/
- Google data center
- https://www.rgj.com/story/money/business/2019/07/31/google-massive-reno-nevada-facility-rising-high-desert/1871965001/
- NCAR : https://www.rgj.com/story/money/business/2019/07/31/google-massive-reno-nevada-facilty-rising-high-desert/1871965001/

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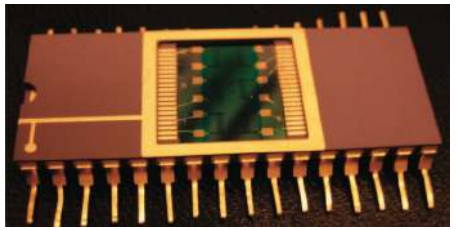
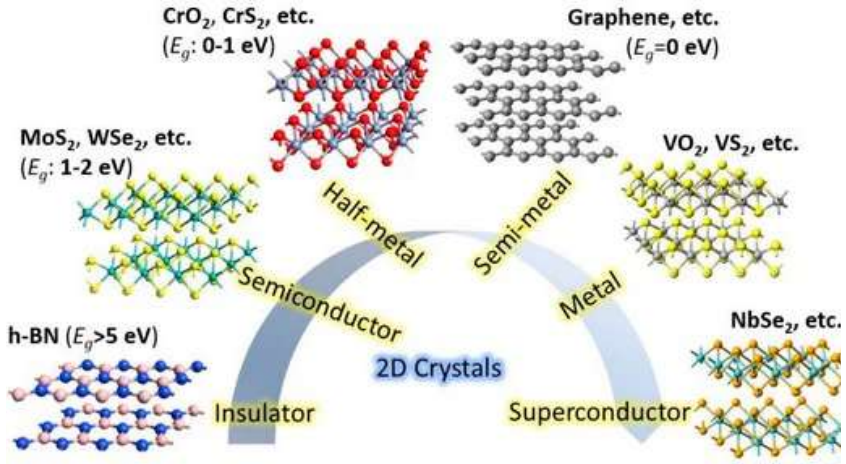
University of Nevada, Reno

Research Areas:
Materials, Sensors and Devices



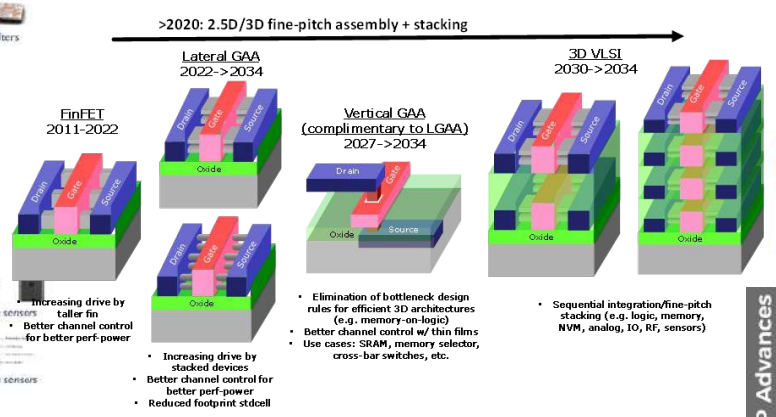
Novel Materials

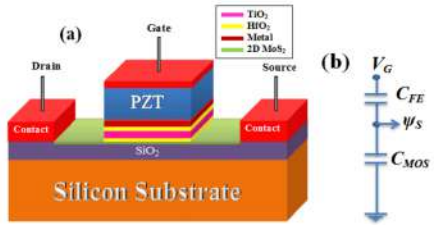


Personal care

Medical applications

Novel Devices





AIP Advances

$HfO_2/TiO_2/HfO_2$ tri-layer high-K gate oxide based MoS_2 negative capacitance FET with steep subthreshold swing

Cite as: AIP Advances 10, 035202 (2020); https://doi.org/10.1063/1.5141939
Submitted: 05 January 2020 . Accepted: 14 February 2020 . Published Online: 02 March 2020

Md. Sherajul Islam, Shahrukh Sadman, A. S. M. Jannatul Islam, and Jeongwon Park

COLLECTIONS

Received: 6 January 2020 | Revised: 26 March 2020 | Accepted: 1 May 2020
DOI: 10.1002/mmce.22291
RESEARCH ARTICLE
INTERNATIONAL JOURNAL OF RF AND MICROWAVE COMPUTER-AIDED ENGINEERING
WILEY

New small-signal extraction method applied to GaN HEMTs on different substrates

Mohamad Al Sabbagh[1] | Mustapha C. E. Yagoub[1] | Jeongwon Park[1,2]

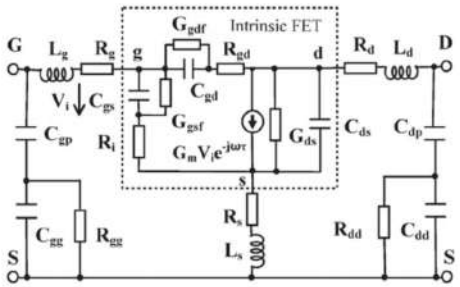


FIGURE 1 GaN HEMT equivalent circuit-small signal model (EC-SSM) including the substrate-buffer model[19]

Agenda

- Introduction
- Semiconductor Market and R&D Trends
- Transistor Scaling
- Challenges and Prospects

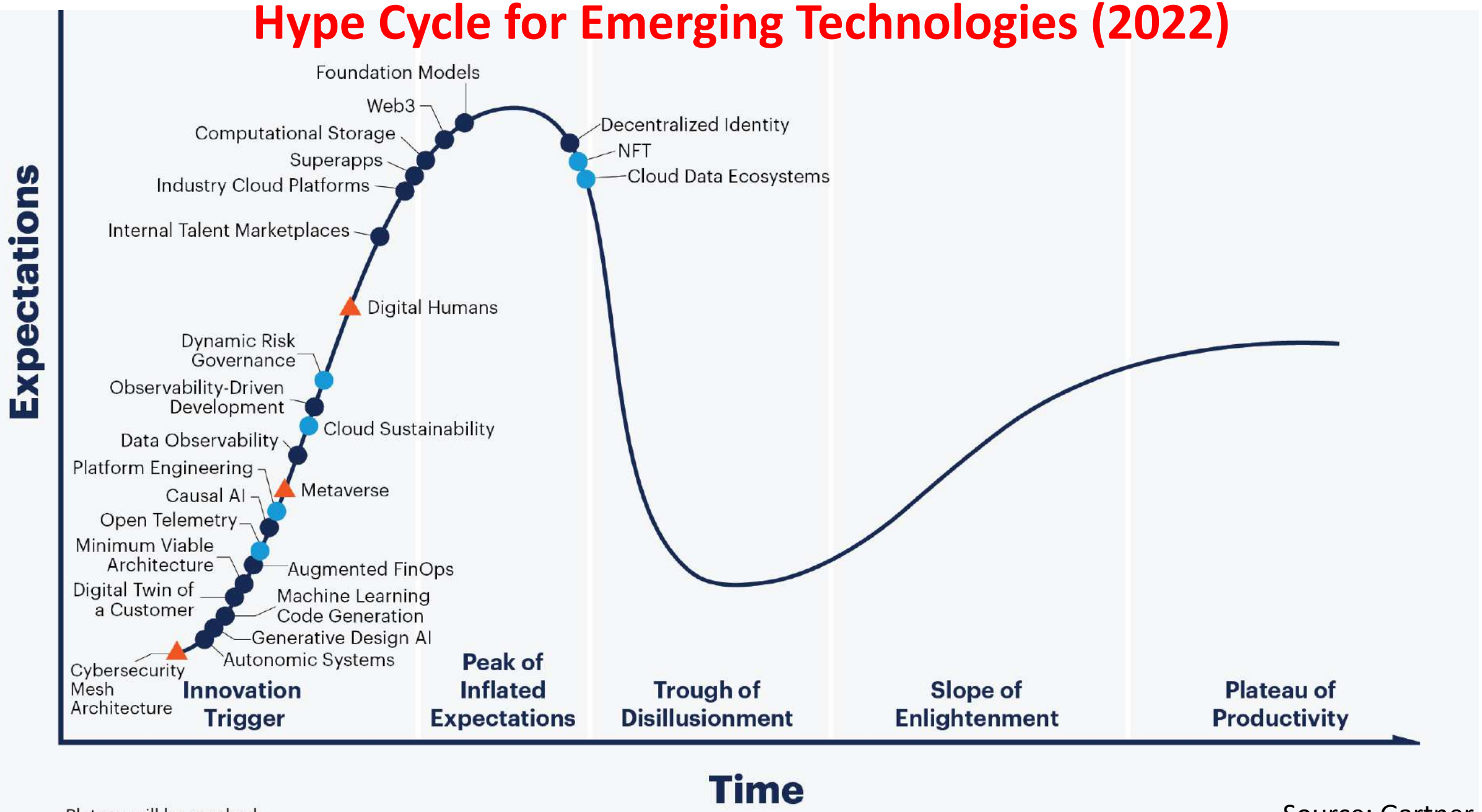
Funding details of CHIPS and Science Act (USD).		
Key Programs	**Five-Year Authorization**	**Increase over Baseline**
National Science Foundation (NSF)	**$81 billion**	**$36 billion**
NSF Tech Directorate	$20 billion	$20 billion
NSF Core activities	$61 billion	$16 billion
Department of Commerce (DOC)	**$11 billion**	**$11 billion**
Regional Technology Hubs	$10 billion	$10 billion
RECOMPETE pilot	$ 1 billion	$ 1 billion
National Institute of Standards and Technology (NIST)	**$10 billion**	**$ 5 billion**
NIST research	$6.9 billion	$2.8 billion
Manufacturing USA	$829 million	$744 million
Manufacturing Extension Partnership	$2.3 billion	$1.5 billion
Department of Energy (DOE)*	**$67.9 billion**	**$30.5 billion**
DOE Office of Science	$50.3 billion	$12.9 billion
Additional DOE Science and Innovation	$17.6 billion	$17.6 billion
Total	**$169.9 billion**	**$82.5 billion**

*Across all the DOE sections, there is:

- A total of $14.7 billion for infrastructure, equipment, and instrumentation across 17 DOE National Laboratories.
- A total of $16.5 billion in new or above baseline authorizations for research in the 10 technology areas identified in the United States Innovation and Competition Act of 2021 across the Office of Science and DOE's applied R&D offices in advanced energy and industrial efficiency technologies, artificial intelligence and machine learning, advanced manufacturing, cybersecurity, biotechnology, high performance computing, advanced materials, and quantum information science.

Source: H.R. 4346, The CHIPS and Science Act of 2022, http://www.commerce.senate.gov.

Hype Cycle for Emerging Technologies (2022)



Source: Gartner

What is Exascale and Why Zettascale

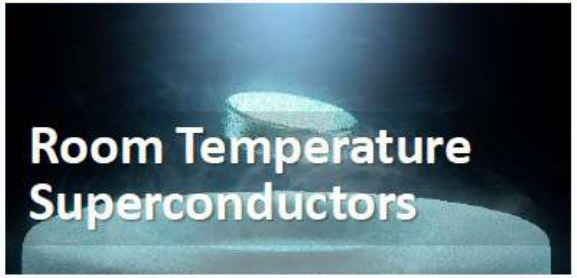
Performance (FP64-tensor)
> 1 Exaflop

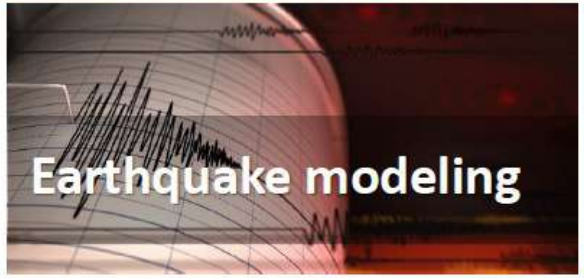
Performance (FP32 -tensor)
> 1 Exaflop

Peak Performance (BF16/Int8 -tensor)
> 8-16 Exaflop

Power
20-30 MW/Exaflop

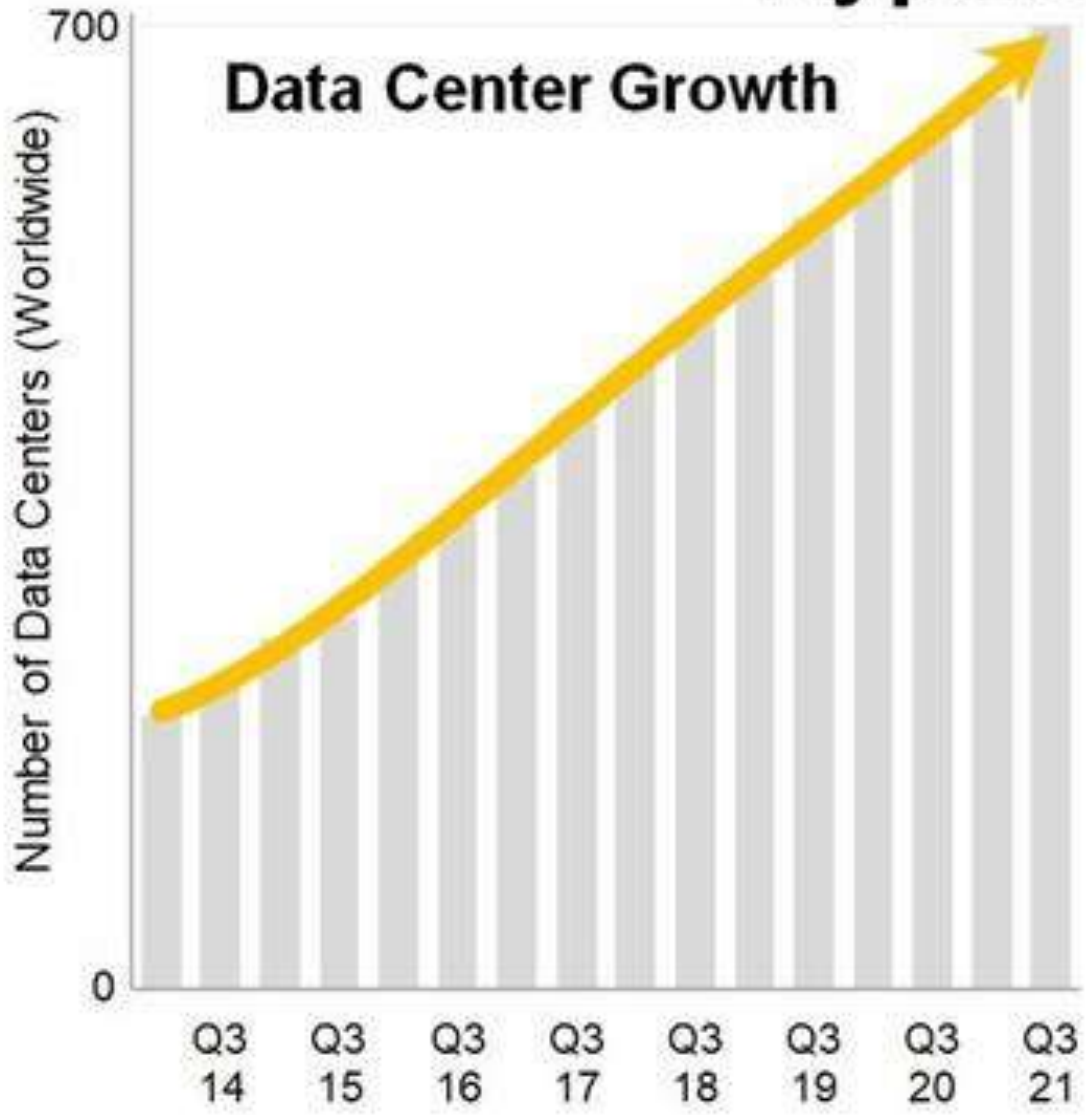
Goal: Solve fundamental problems from first principles

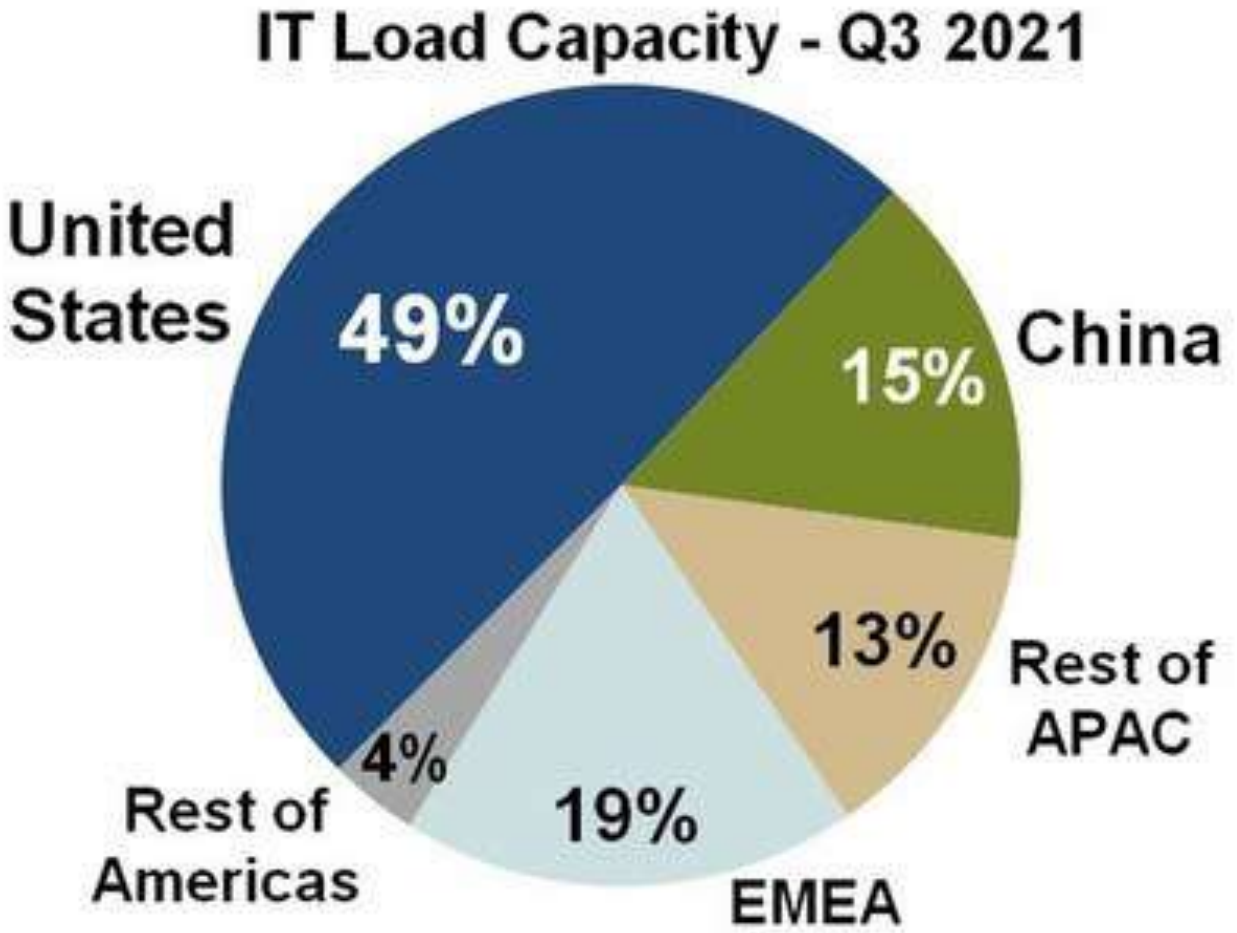




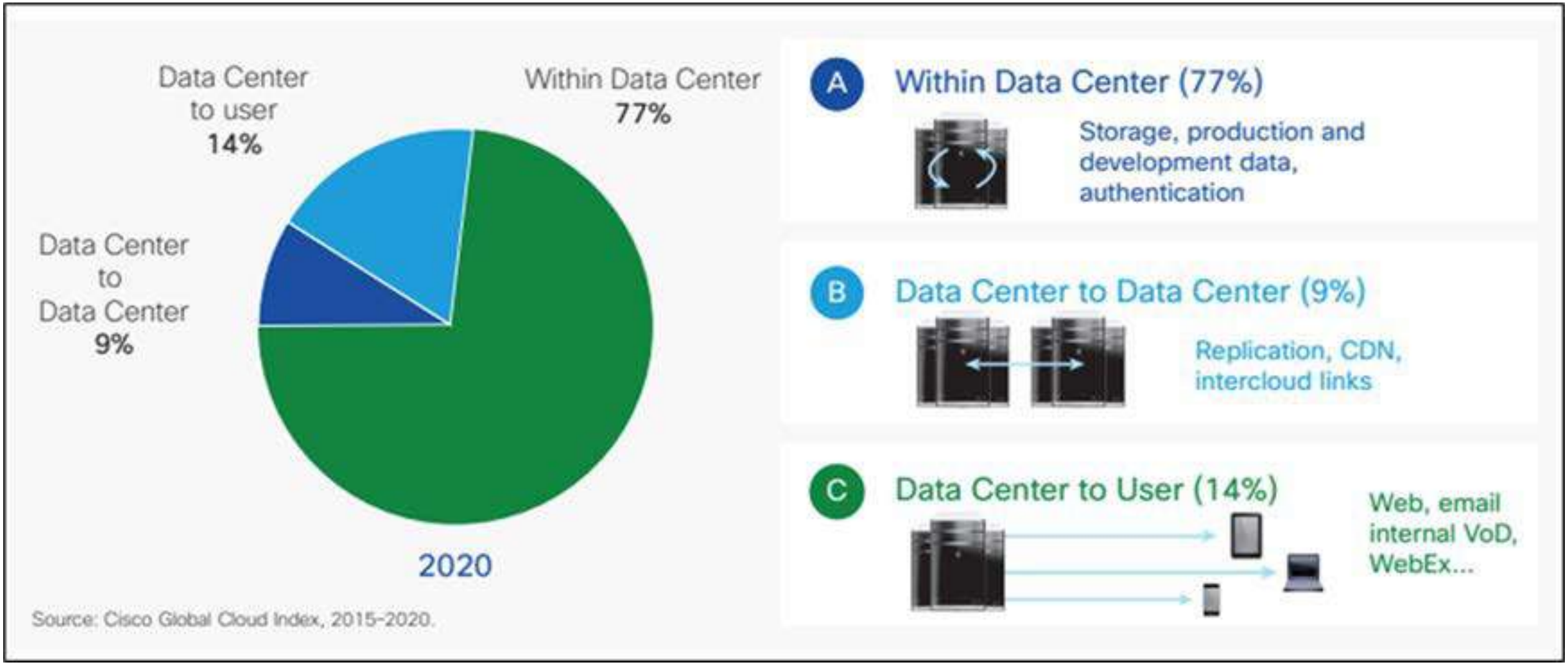
Zettascale technologies will make Exascale mainstream

Hyperscale Data Centers



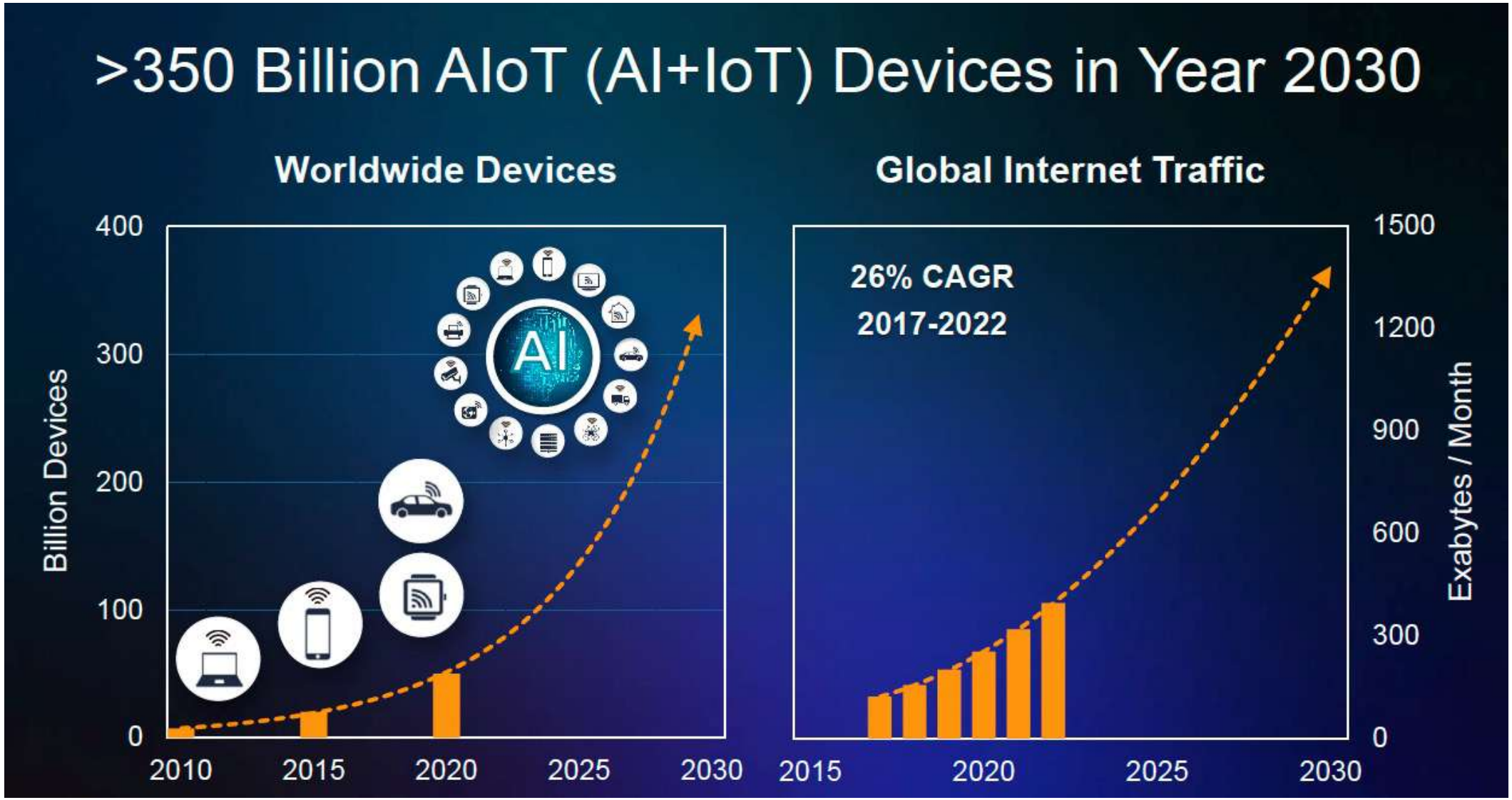


Source: Synergy Research Group



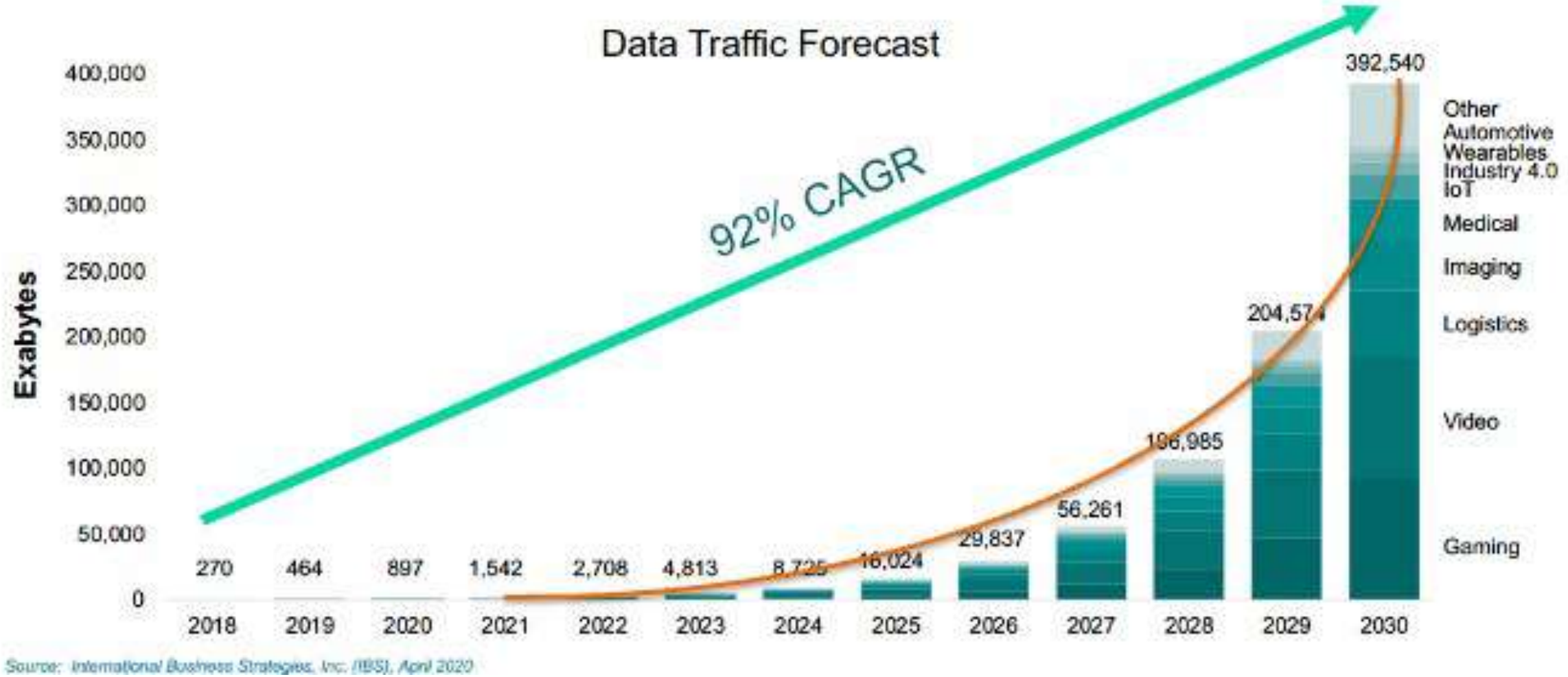
Traffic within data center is main limiting factor

Demand for higher data rates concurrently fueling demand of billions of devices



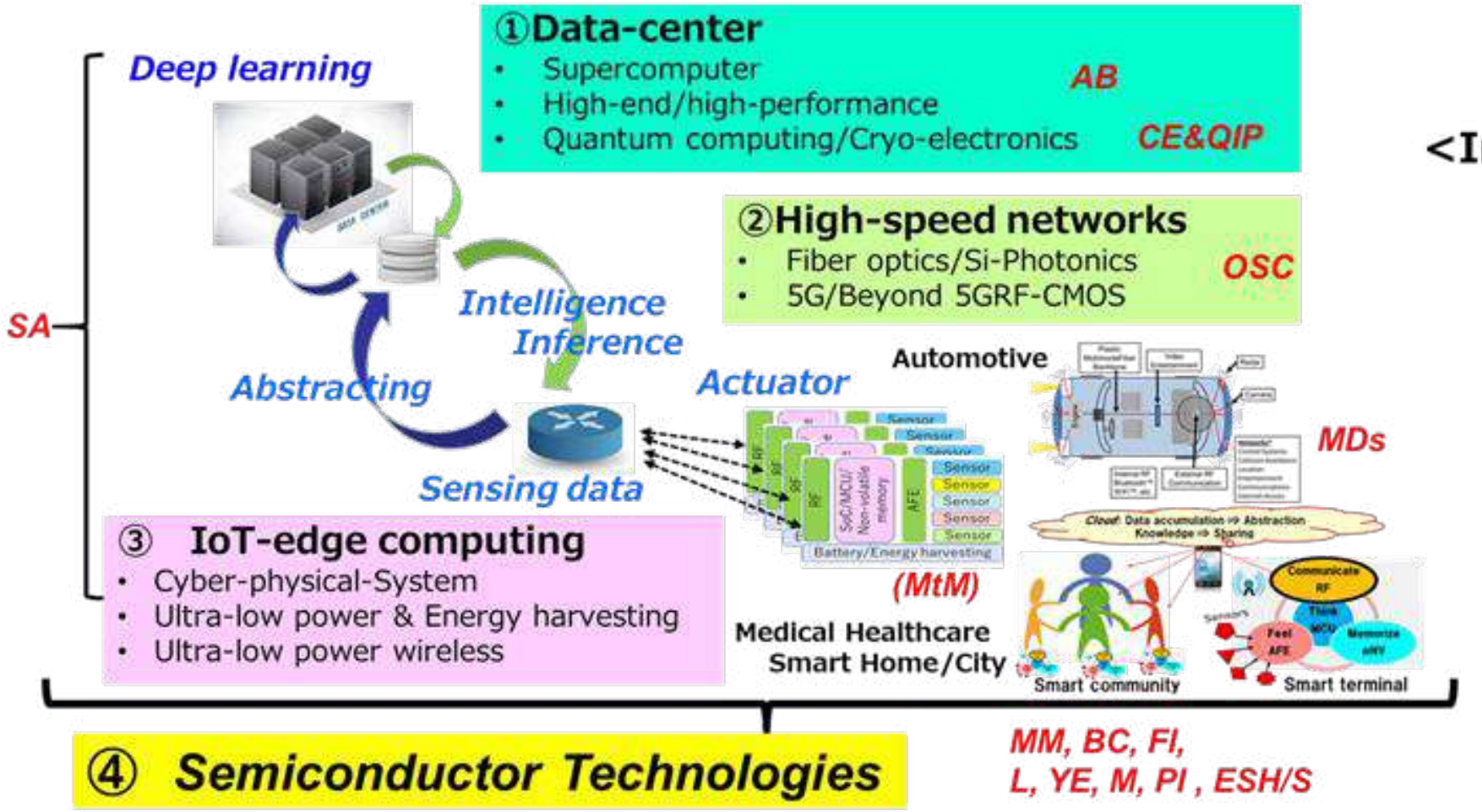
Source: 2020 IEEE ISSCC, Cisco VNI Global IP Traffic Forecast 2017-2022

Exponential data traffic, enabled by machine-to-machine communication



Source: International Business Strategies, Inc. (IBS), April 2020

The new ecosystem of the electronics' industry based on semiconductor technologies.



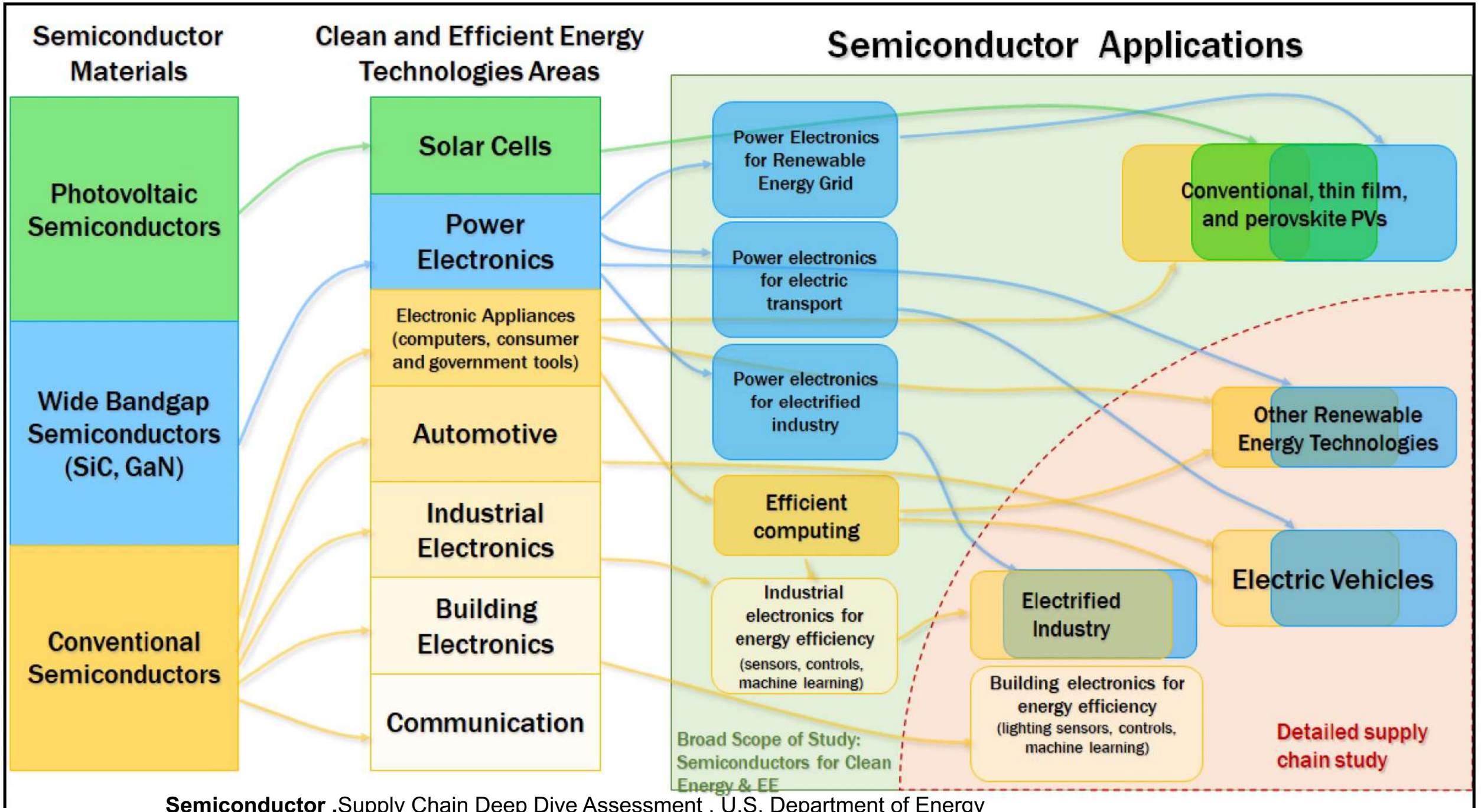
<International Collaboration>

International Roadmap Committee (IRC@2020.6)

- IEEE IRDS™
- SDRJ/JSAP*1
- SINANO*2 institute

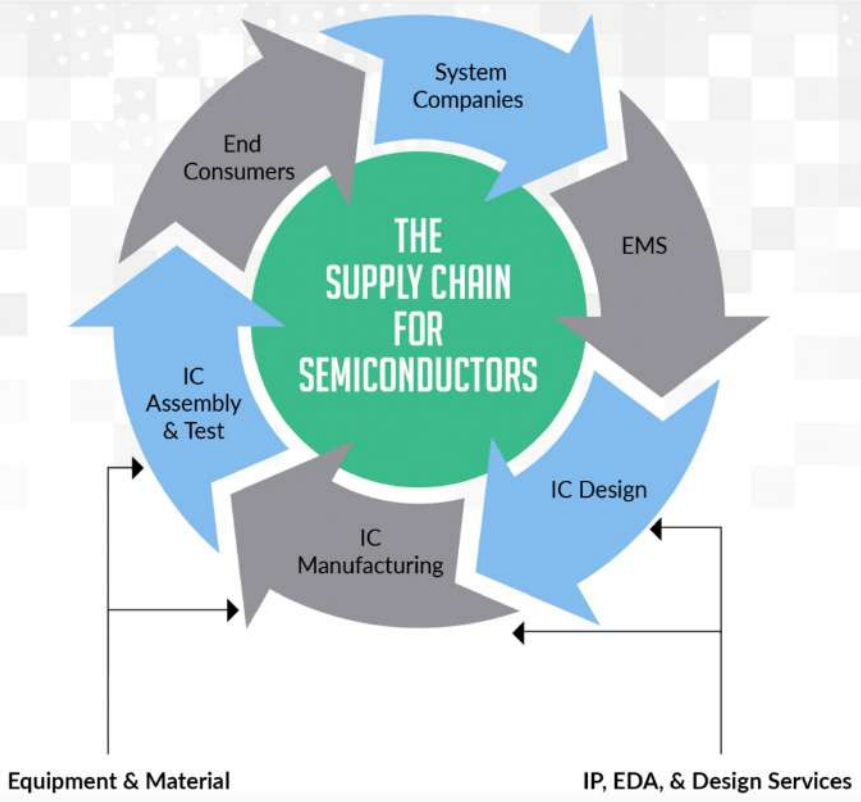
AB: Applications Benchmarking, ***SA***: Systems and Architecture, ***OSC***: Outside system Connectivity, ***MM***: More Moore, ***BC***: Beyond CMOS, ***CE&QIP***: Cryogenics Electronics and Quantum Information Processing, ***PI***: Packaging Integration, ***FI***: Factory Integration, ***L***: Lithography, ***YE***: Yield Enhancement, ***M***: Metrology, ***ESH/S***: Environment, Safety, Health, and Sustainability, ***MtM***: More than Moore, ***MDs***: Market drivers (automobile, medical devices).

*1: The System Device Roadmap Committee of Japan/The Japan Society of Applied Physics
*2: The European Academic and Scientific Association for Nanoelectronics

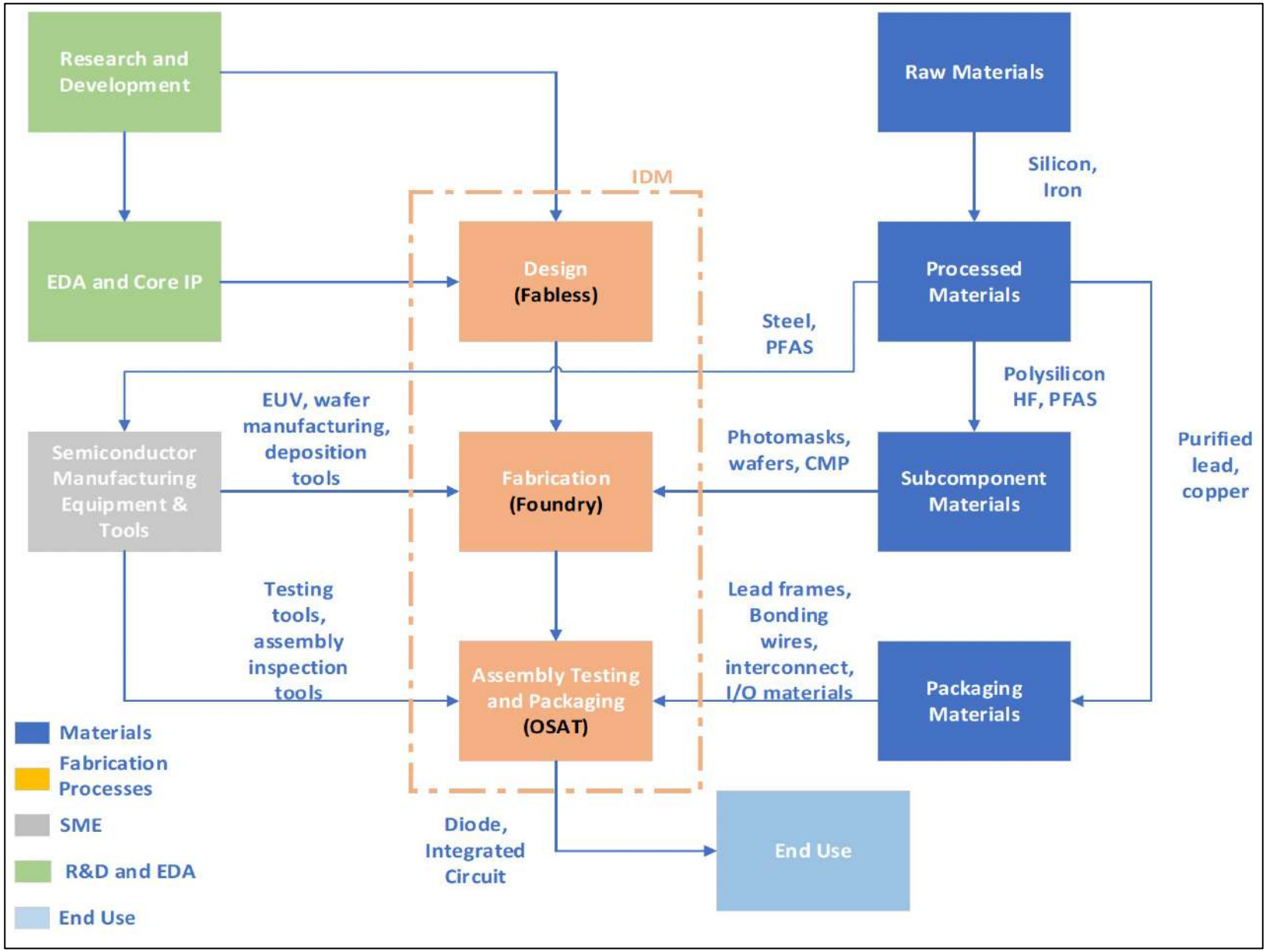


Semiconductor ,Supply Chain Deep Dive Assessment , U.S. Department of Energy
Response to Executive Order 14017, “America’s Supply Chains” ,February 24, 2022

Semiconductor Value Chain

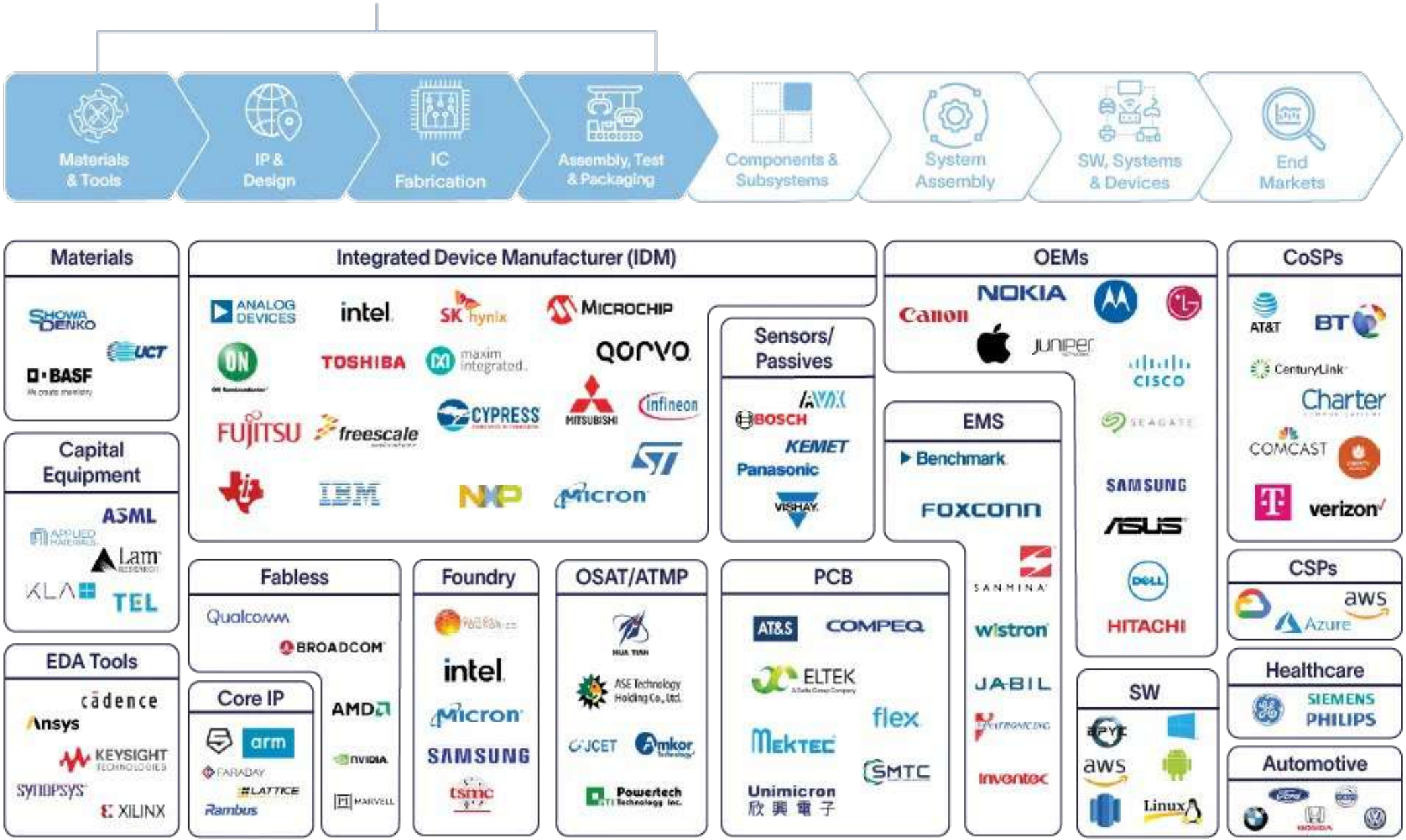


Source: TSMC



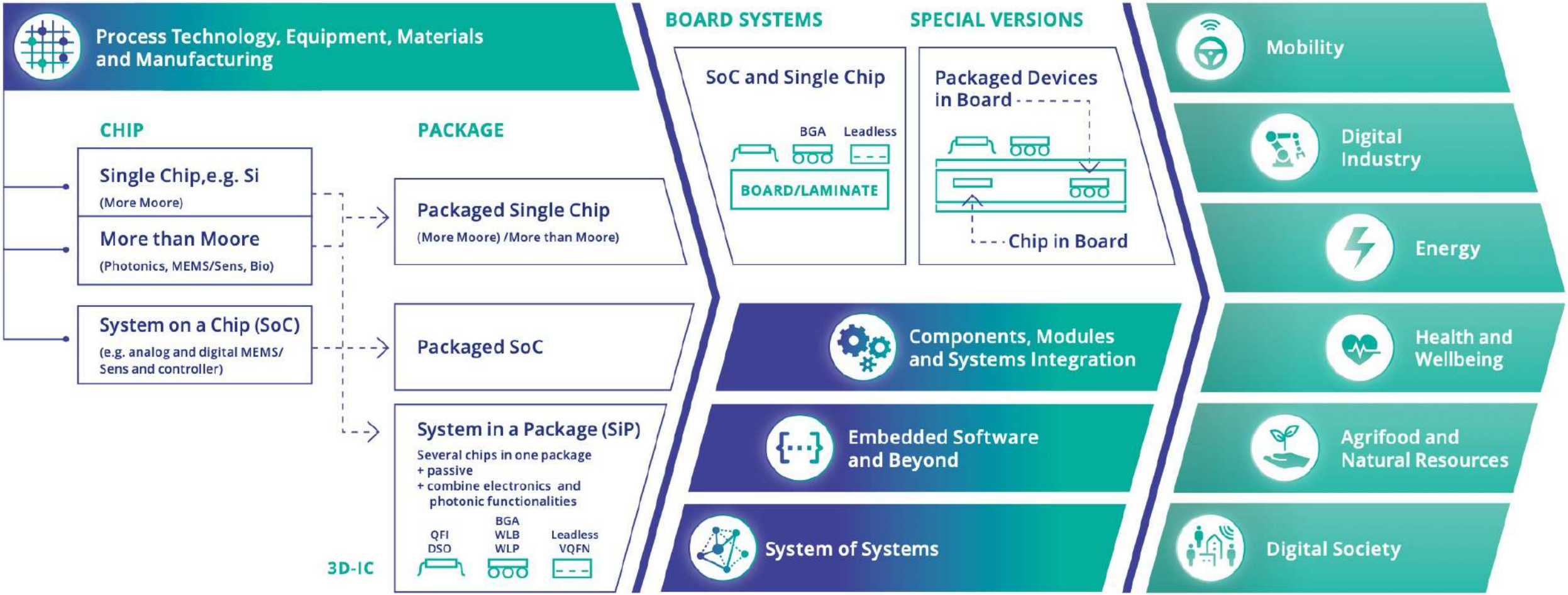
Semiconductor ,Supply Chain Deep Dive Assessment , U.S. Department of Energy Response to Executive Order 14017, “America’s Supply Chains” ,February 24, 2022

Semiconductor Value Chain

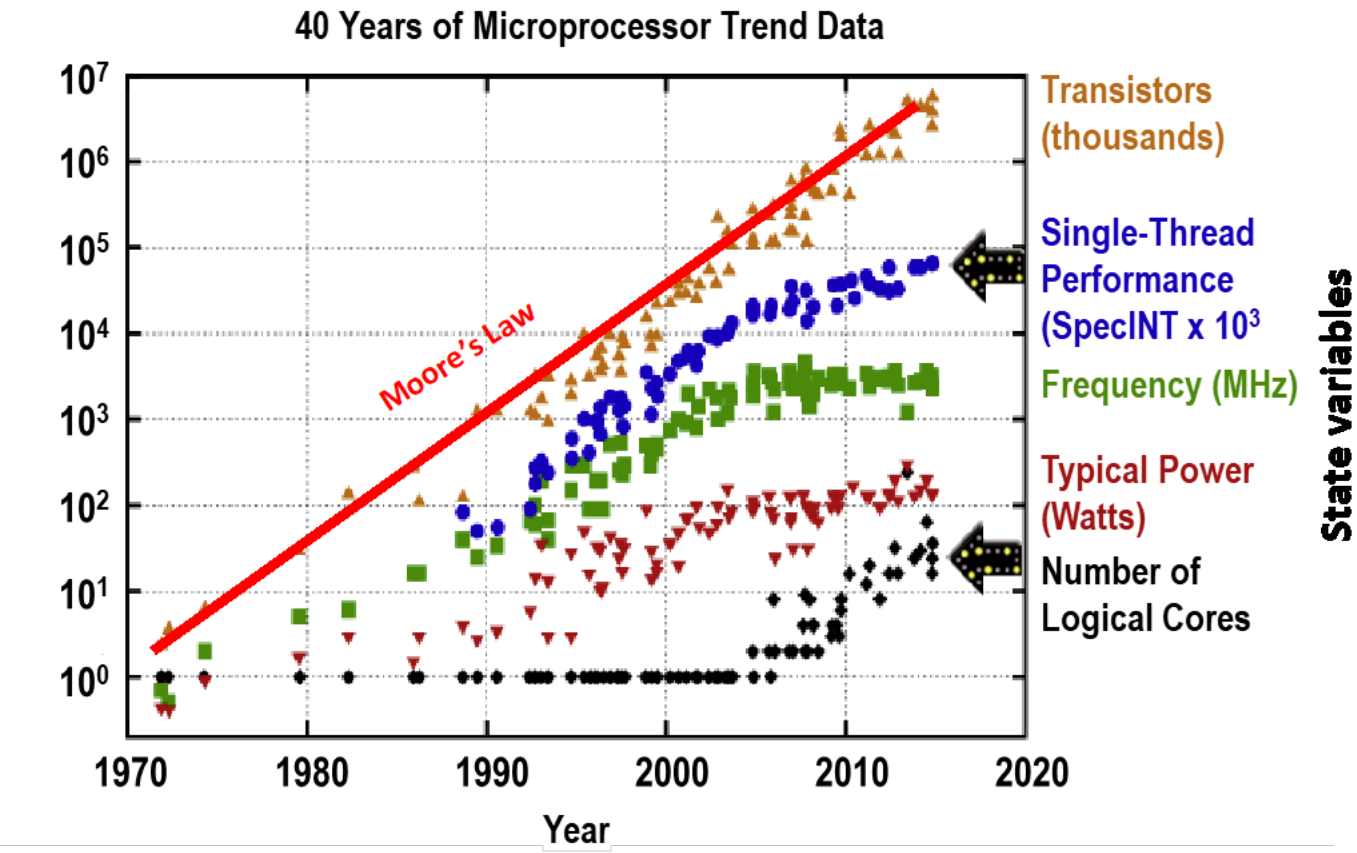


https://www.altmansolon.com/insights/the-semiconductor-ecosystem-complex-global-and-specialized/

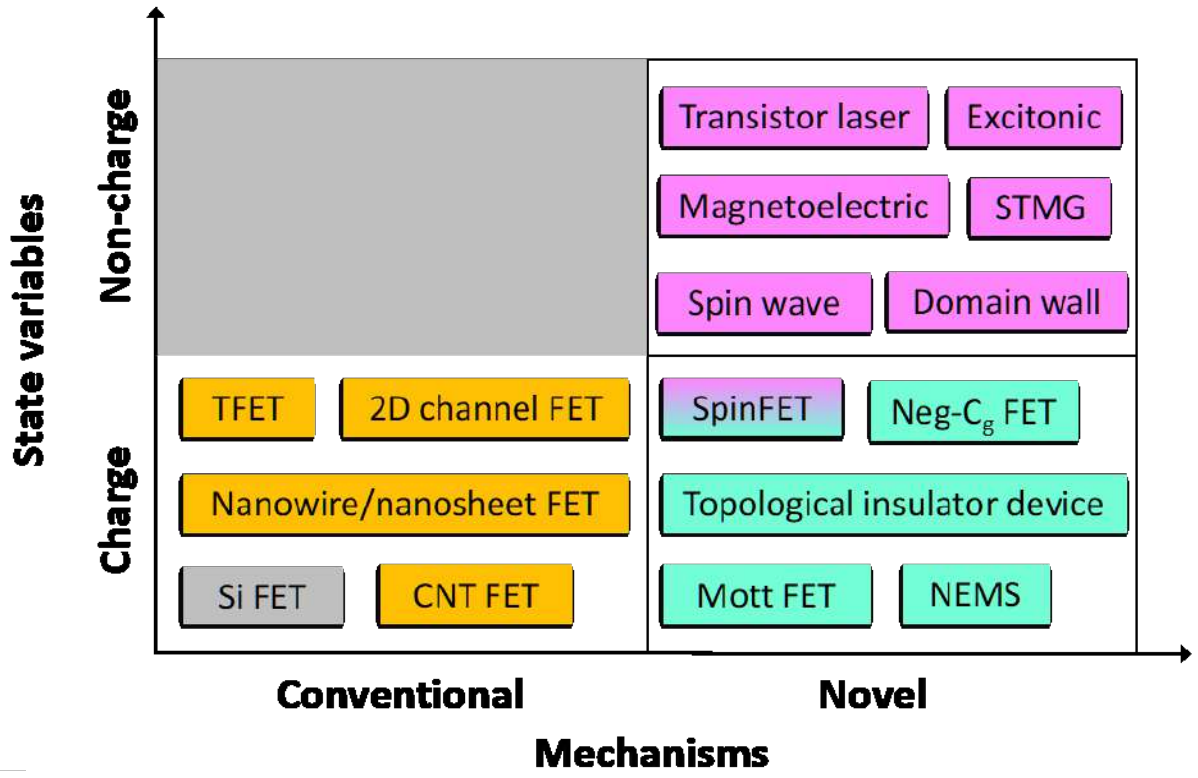
Ecosystem of semiconductors



Nanodevices for Computing and Logic Beyond CMOS



IRDSRoadmap: Devices Beyond CMOS



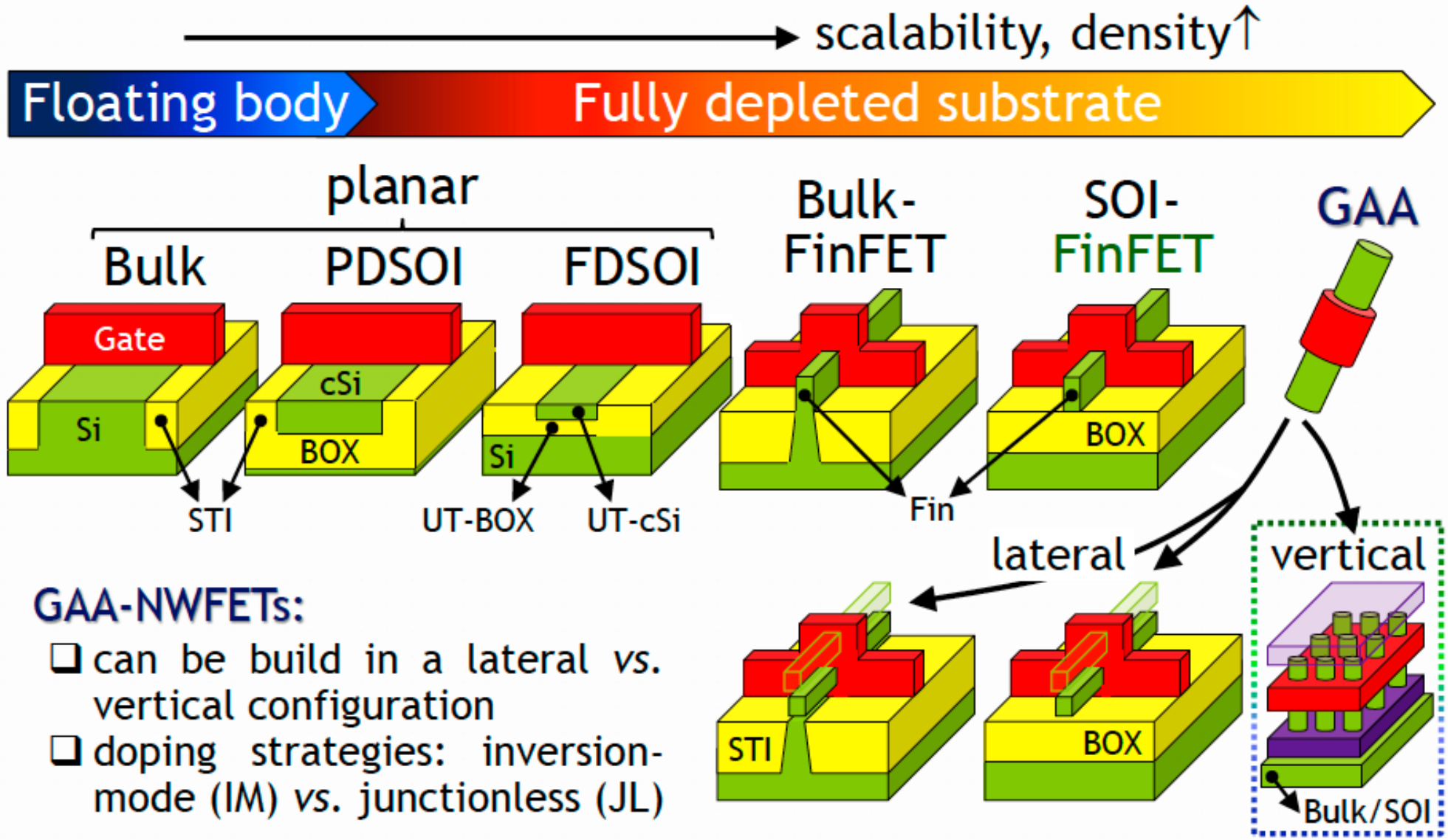
Identify and Mature Options for Semiconductors Beyond the Present State of the Art

Materials to Systems in Semiconductor Manufacturing and Beyond

Semiconductor Manufacturing

Om Nalamasu, Applied Materials, 2021 Symposium on VLSI Technology Digest of Technical Papers

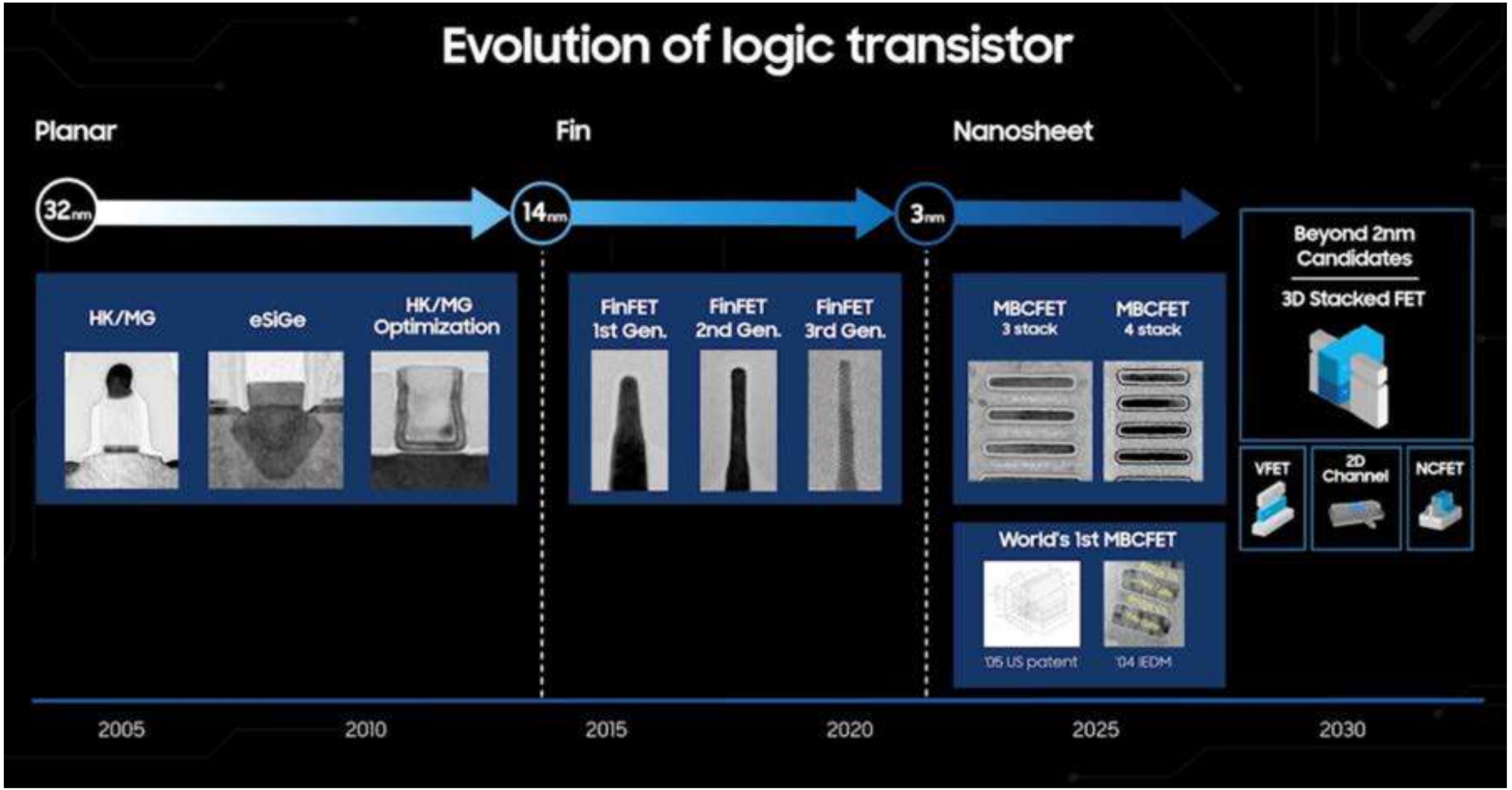
Introduction:
scaling scenario for device architectures



GAA-NWFETs:

- ❑ can be build in a lateral *vs.* vertical configuration
- ❑ doping strategies: inversion-mode (IM) *vs.* junctionless (JL)

Transistor 2003-2025 evolution: From 2D Equivalent scaling to 3D Power scaling

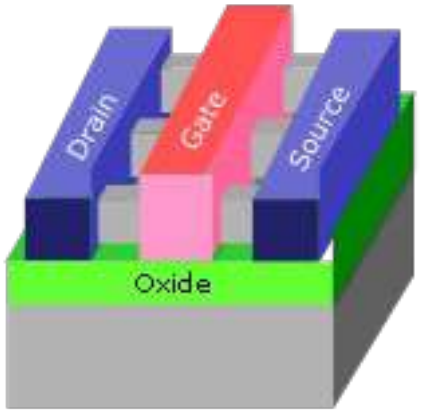


Source: Intel investor meeting 2022

Change in the MOSFET device architecture from the 2D planar through 2.5D FinFets to 3D monolithic VLSI with GAA

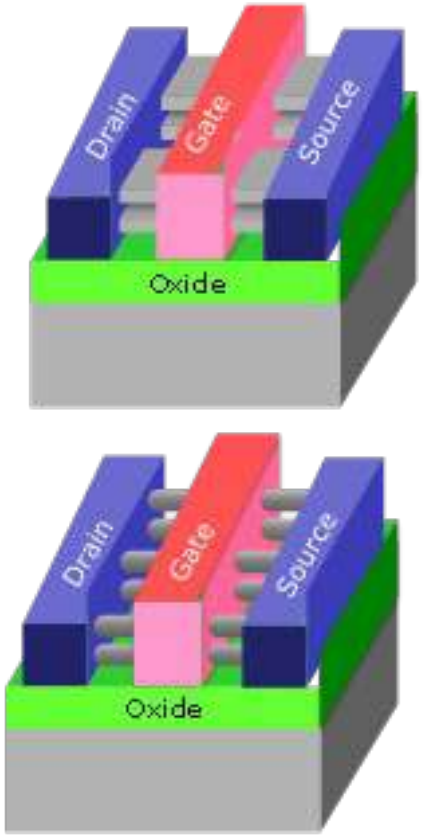
>2020: 2.5D/3D fine-pitch assembly + stacking

FinFET
2011-2022



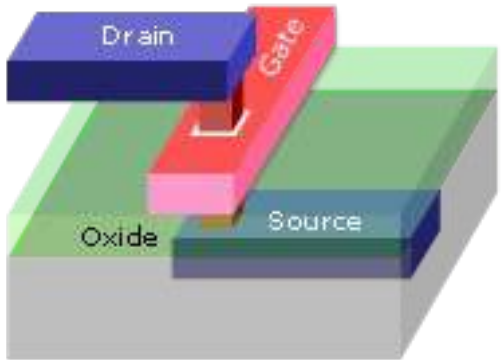
- Increasing drive by taller fin
- Better channel control for better perf-power

Lateral GAA
2022->2034



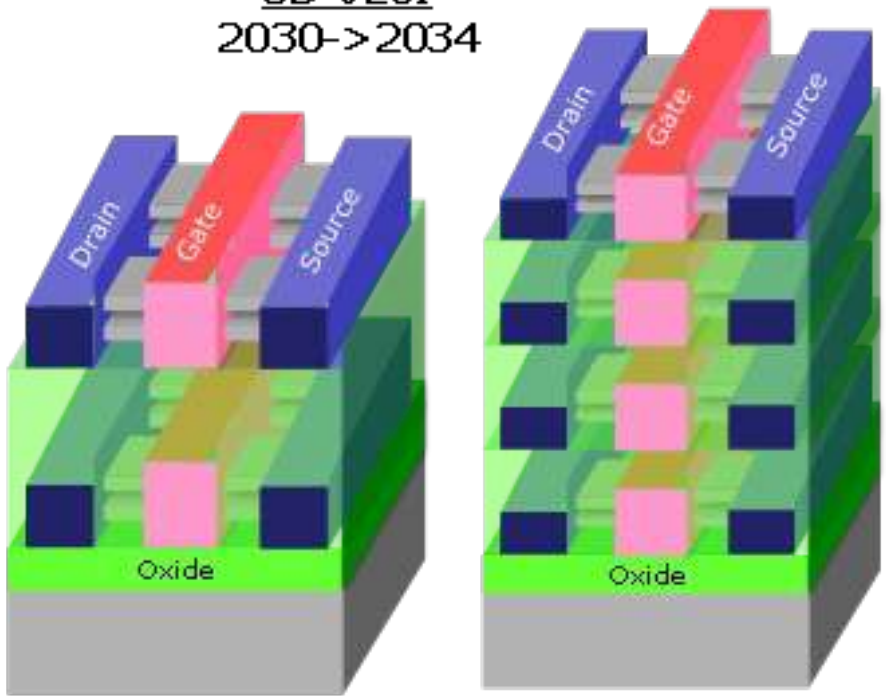
- Increasing drive by stacked devices
- Better channel control for better perf-power
- Reduced footprint stdcell

Vertical GAA
(complimentary to LGAA)
2027->2034



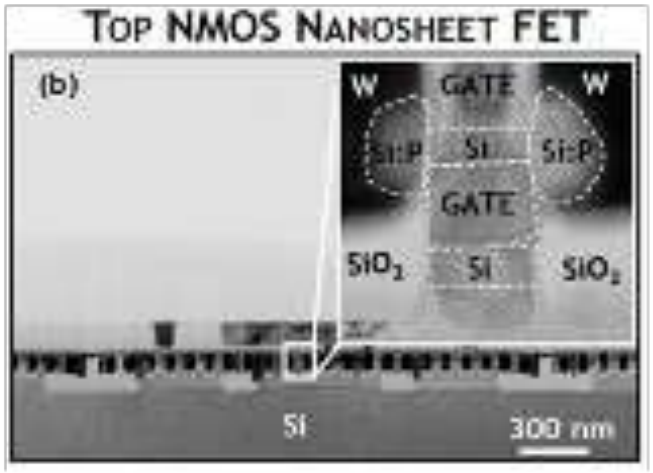
- Elimination of bottleneck design rules for efficient 3D architectures (e.g. memory-on-logic)
- Better channel control w/ thin films
- Use cases: SRAM, memory selector, cross-bar switches, etc.

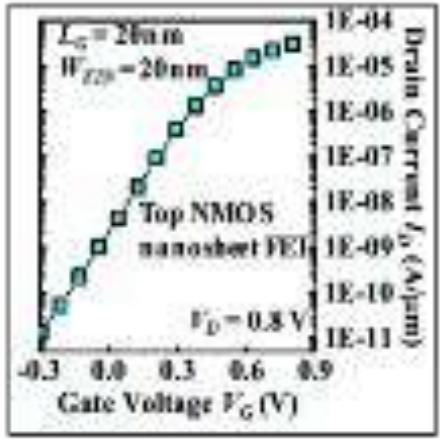
3D VLSI
2030->2034

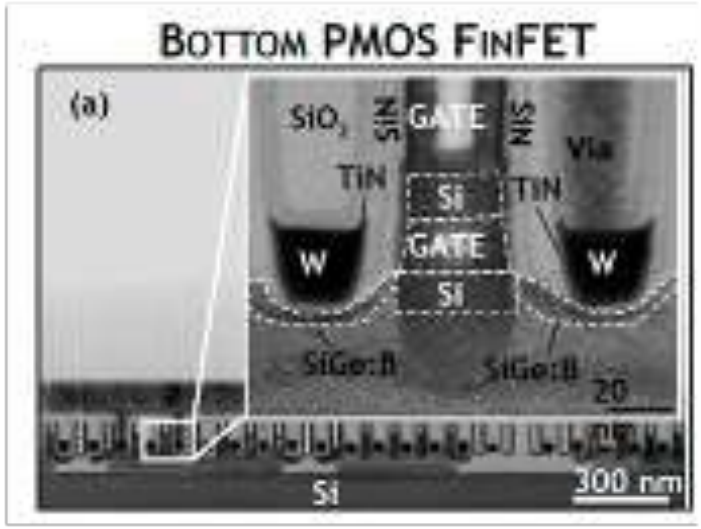


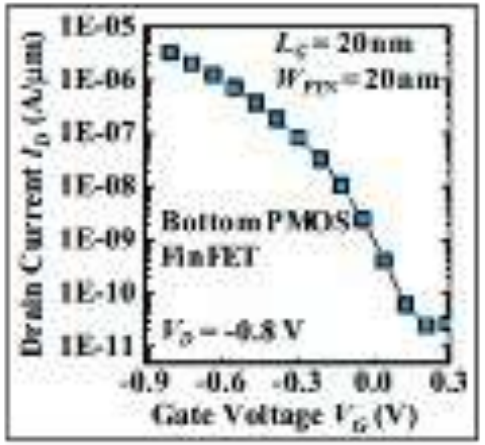
- Sequential integration/fine-pitch stacking (e.g. logic, memory, NVM, analog, IO, RF, sensors)

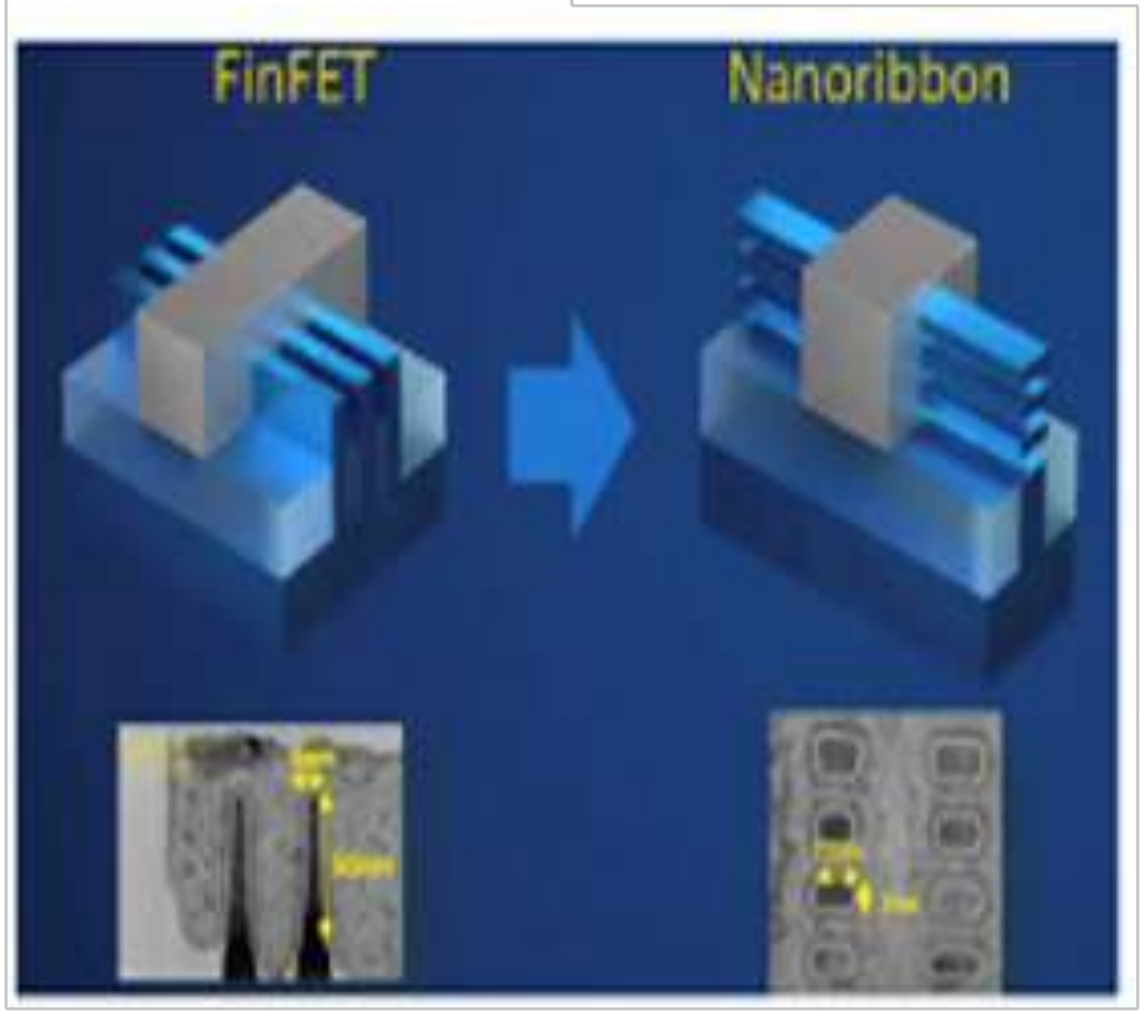
Vertical transistors and nanoribbons are progressively entering the logic technology arsenal



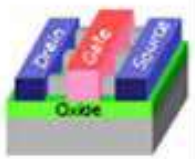
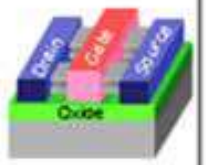
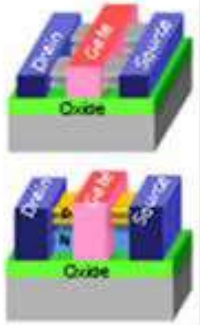
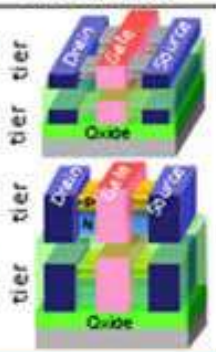
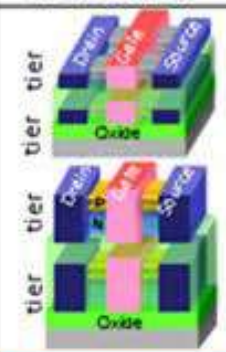
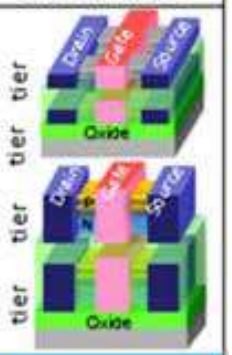








Source: IMEC and Intel

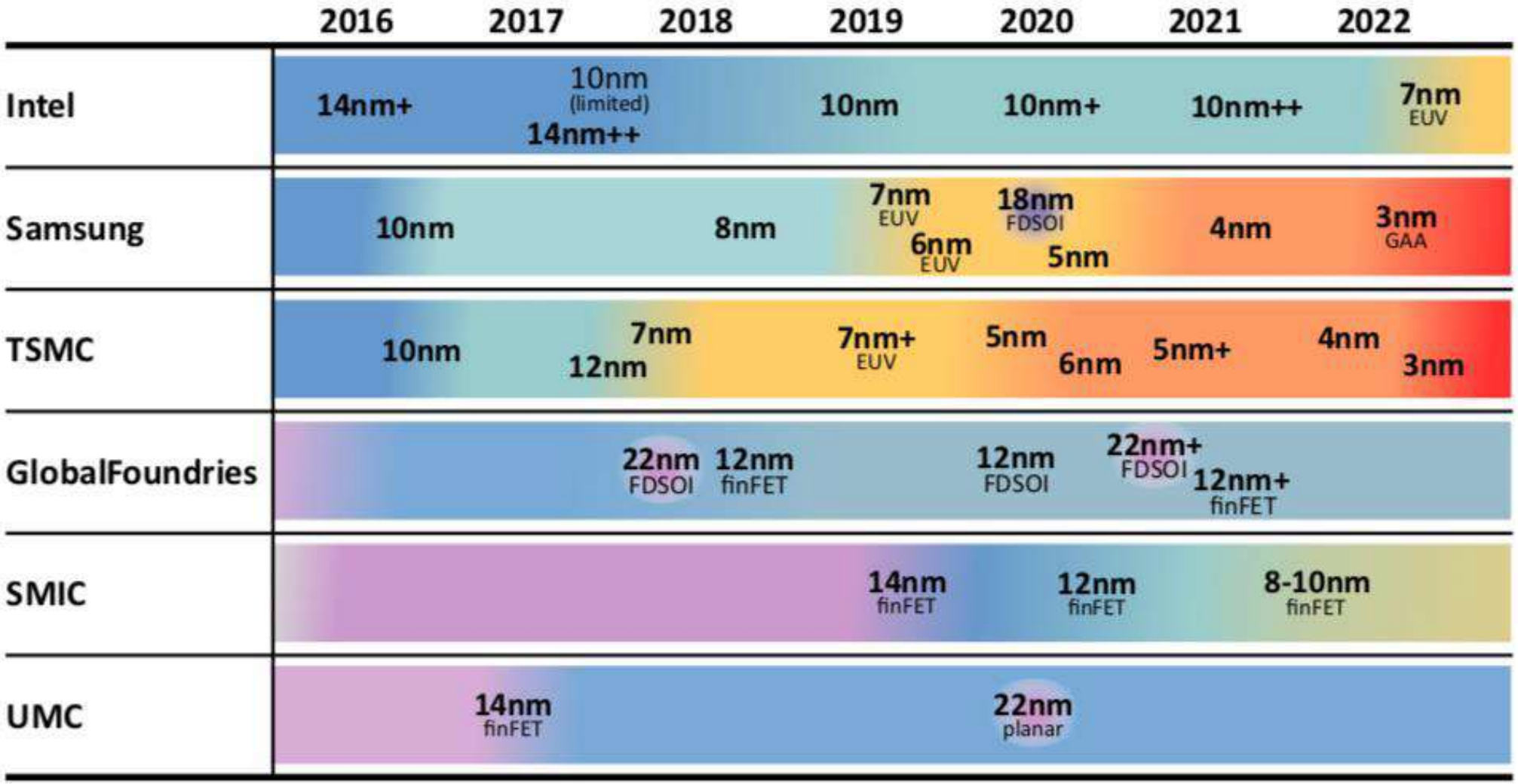
YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16 T2	G38M16 T4	G38M16 T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length - HP (nm)	16	14	12	12	12	12
Lg: Gate Length - HD (nm)	18	14	12	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency - finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) - HP		30	30	20	15	15
LGAA width (nm) - HD		15	10	10	6	6
LGAA width (nm) - SRAM		7	6	6	6	6
Footprint drive efficiency - lateral GAA - HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) - HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) - HD	101.0	126.0	96.0	128.0	88.0	80.0
PN seperation width (nm)	45	40	20	15	15	10

Overall technology progression in the 2022 IRDS remains close to forecast.

YEAR OF PRODUCTION	2021	2022	2025	2028	2031	2034
	G51M30	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Platform device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
Frequency scaling - node-to-node	-	0.02	0.16	0.09	-0.08	-0.01
CPU frequency at constant power density (GHz)	3.13	2.83	3.53	2.50	1.48	0.86
Power at iso frequency - node-to-node	-	-0.16	-0.27	-0.05	-0.06	-0.08
Power density - relative	1.00	1.12	1.04	1.59	2.51	4.27
LOGIC TECHNOLOGY ANCHORS						
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Beyond-CMOS as complimentary to platform CMOS	-	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat
Process technology inflection	Conformal Doping, Contact	Channel, RMG	Lateral/AtomicEtch	Non-Cu Mx	3DVLSI	3DVLSI
Stacking generation inflection	2D	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic	3D-stacking, 3DVLSI: Mem-on-Logic with Interconnect	3D-stacking, 3DVLSI: Logic-on-Logic

Devices will continue to aggressively scale in the next 5 years

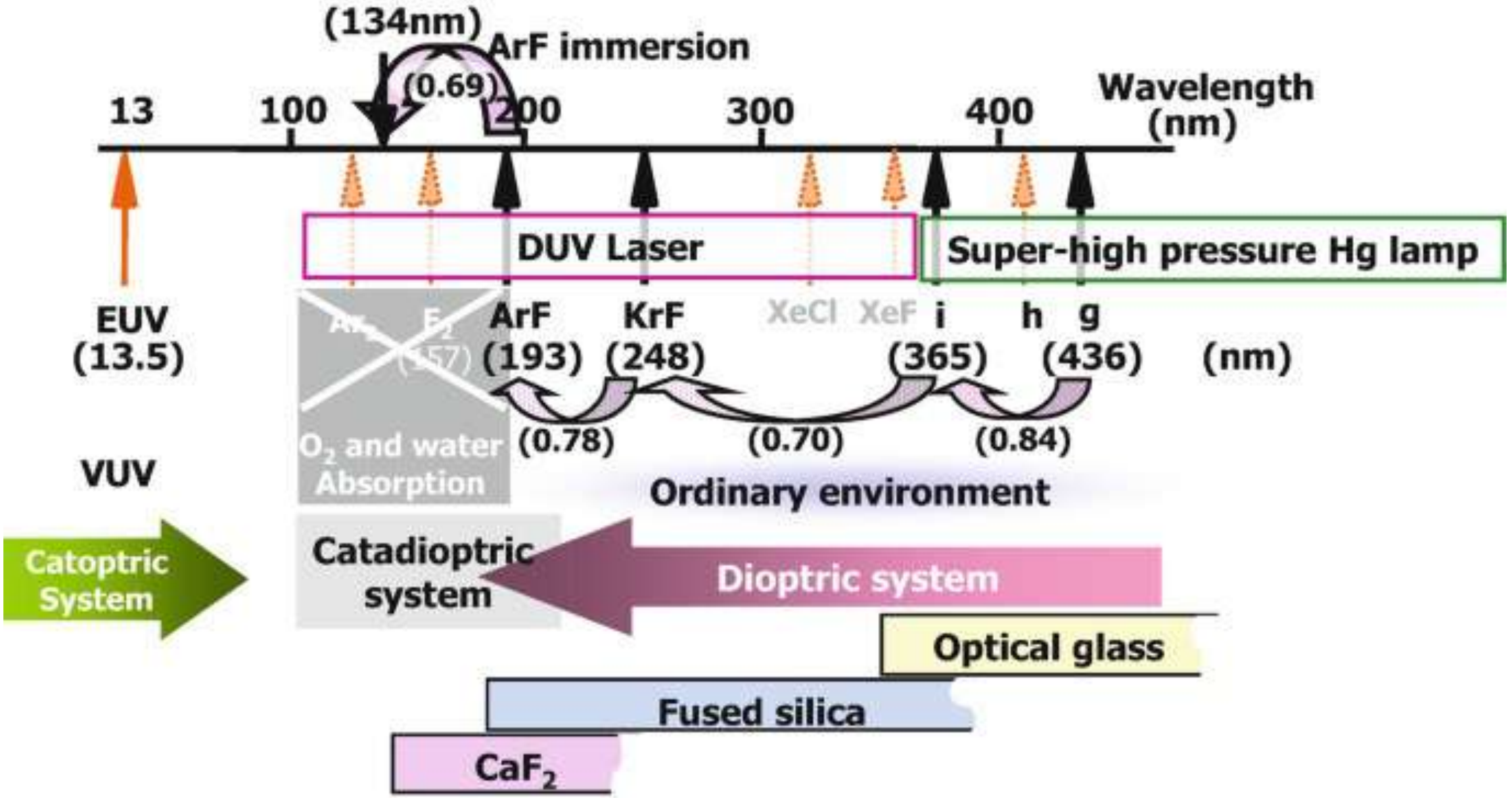
Logic/Foundry Process Roadmaps (for Volume Production)



Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embelishments, so these points of transition should only be seen as very general guidelines.

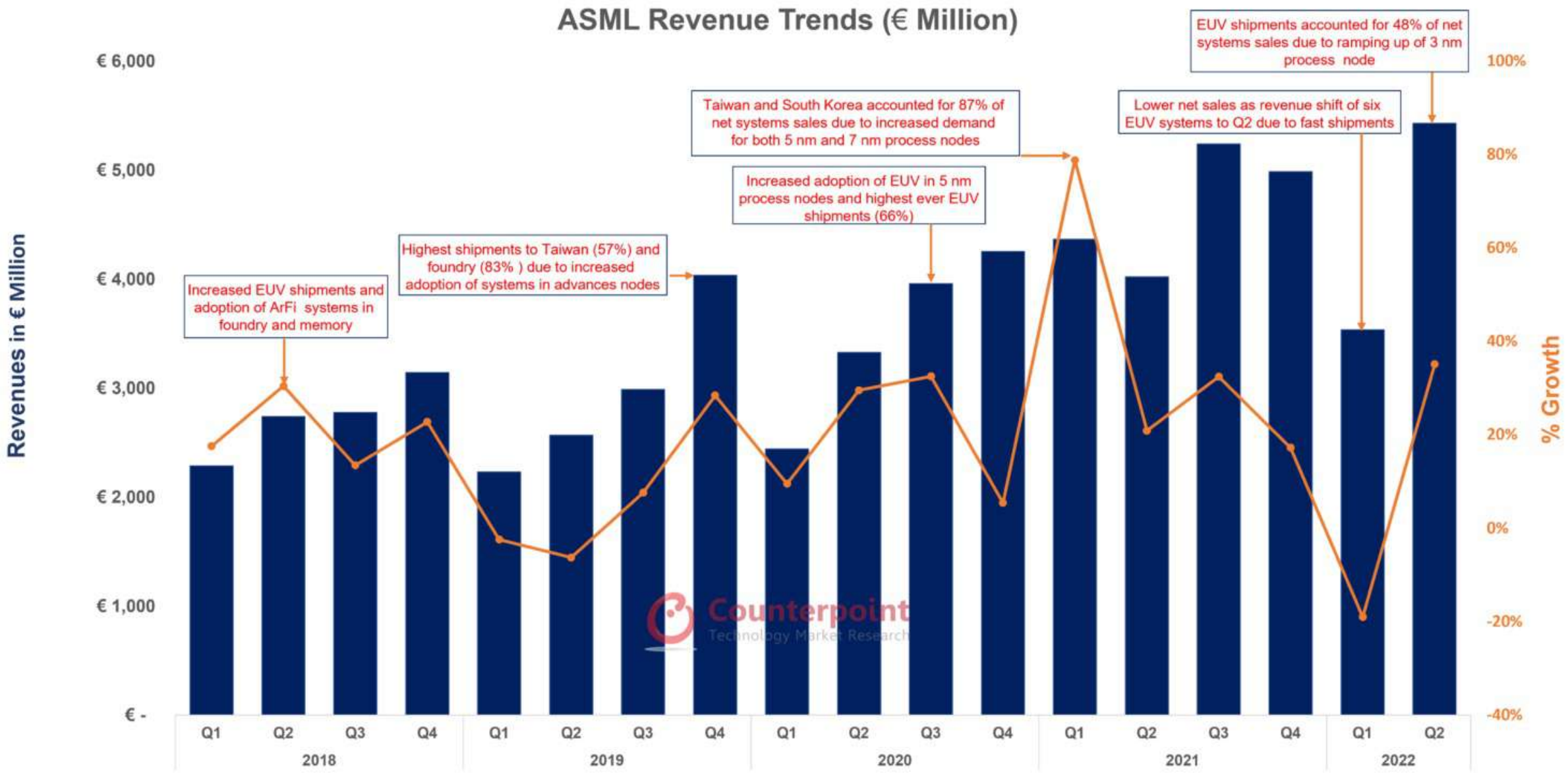
Sources: Companies, conference reports and IC Insights

Lithography scanners



https://www.semianalysis.com/p/the-gaps-in-the-new-china-lithography

Growth of EUV lithography scanners



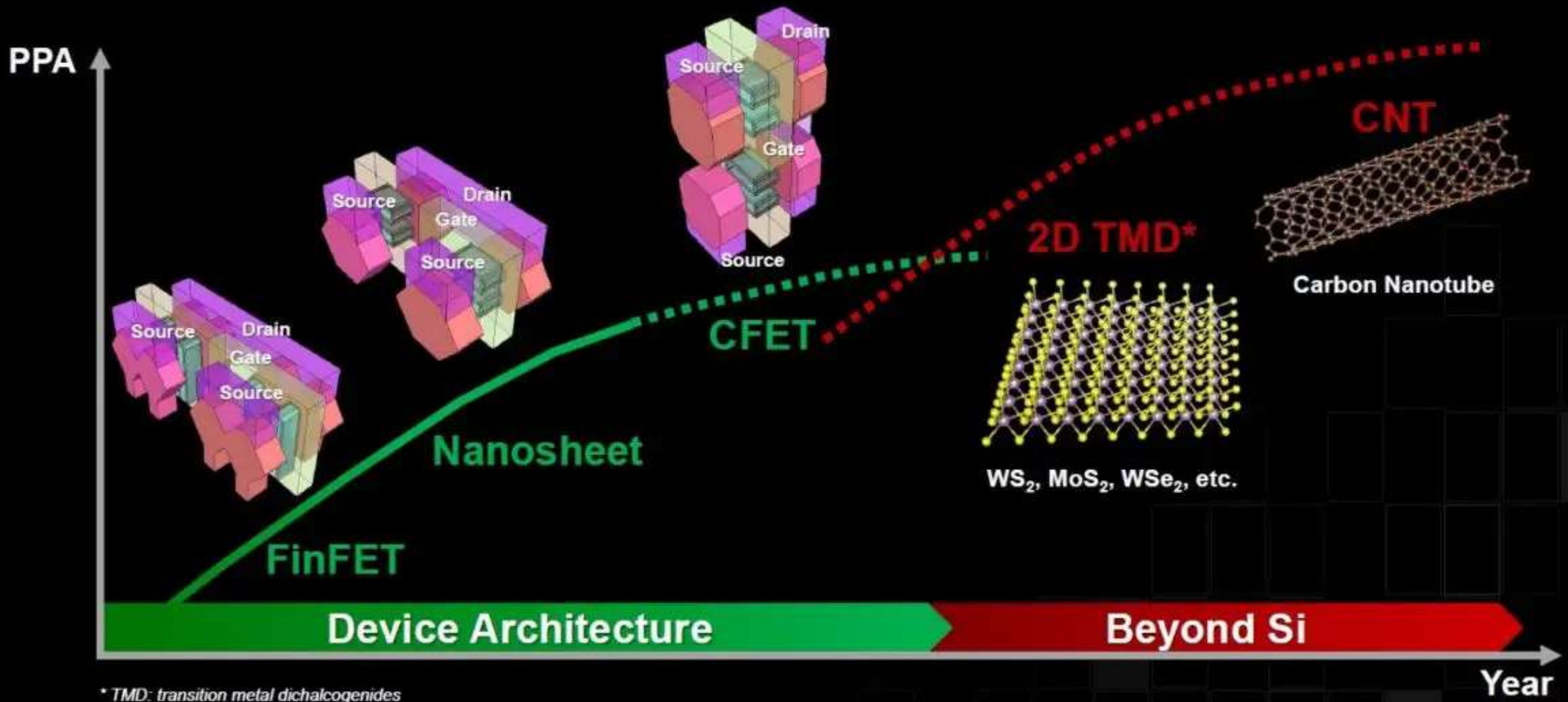
https://www.counterpointresearch.com/increased-euv-shipments-help-asml-deliver-strong-growth-in-q2-2022/

TSMC Advanced Technology Roadmap

Unleash Innovation

https://semiwiki.com/semiconductor-manufacturers/tsmc/328096-tsmc-2023-north-america-technology-symposium-overview-part-1/

Device Architecture Outlook



* TMD: transition metal dichalcogenides

https://semiwiki.com/semiconductor-manufacturers/tsmc/328118-tsmc-2023-north-america-technology-symposium-overview-part-2/

Potential logic scaling roadmap extension

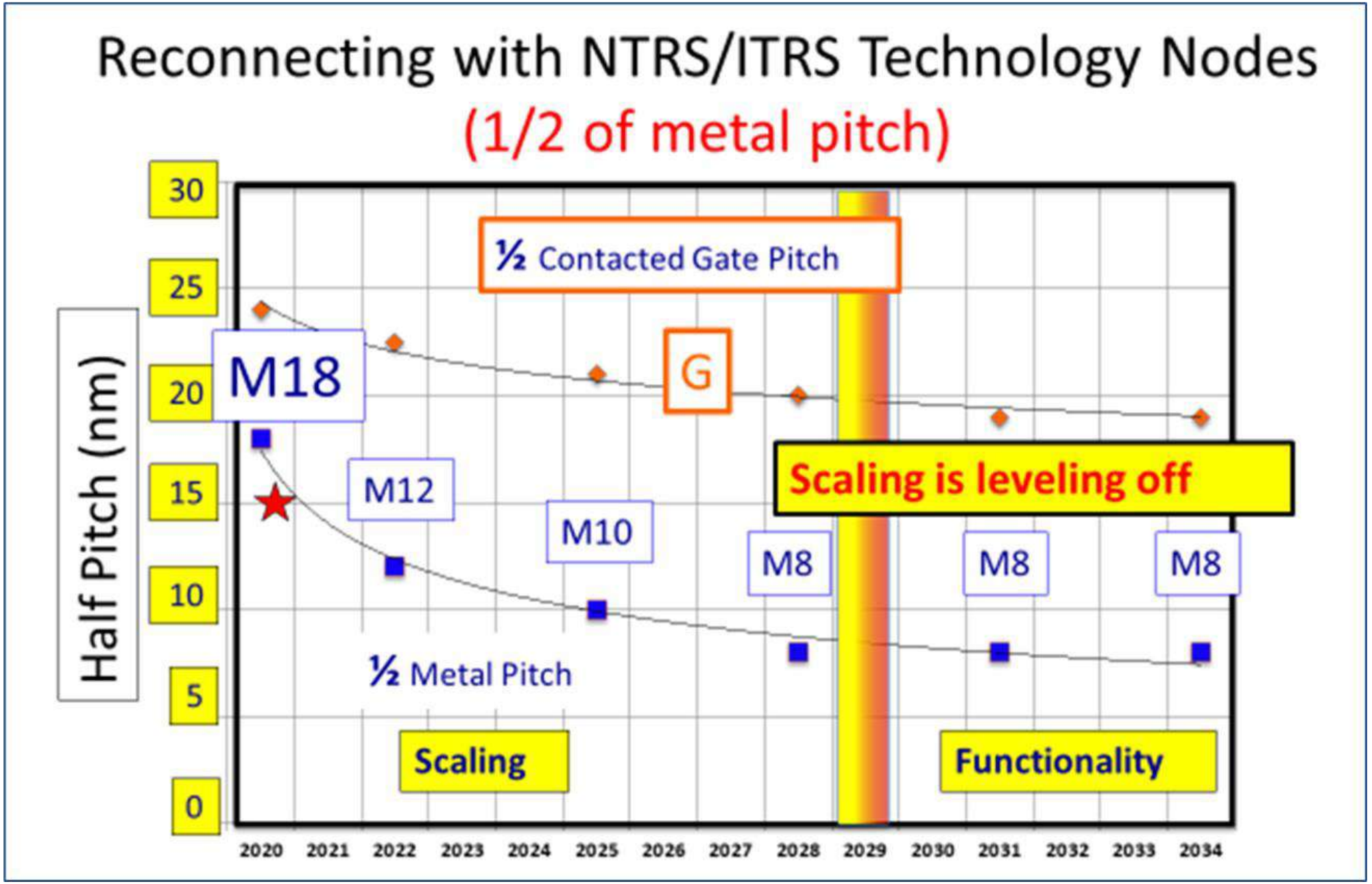
	2018	2020	2022	2024	2026	2028	2030	2032	2034	2036
	N7	N5	N3	N2	A14	A10	A7	A5	A3	A2
Metal Pitch (nm)	40	28	21	21	18	18	16	16	16	16-12
							Continued dimensional scaling			
Metal Tracks	6	6	6	6	5	5	5	4	<4T	<4T
	finFET	finFET	finFET	GAA NSFET	GAA NSFET	FSFET	FSFET	CFET	CFET	CFET atomic
							Device and material innovations			

Context-aware interconnect

imec

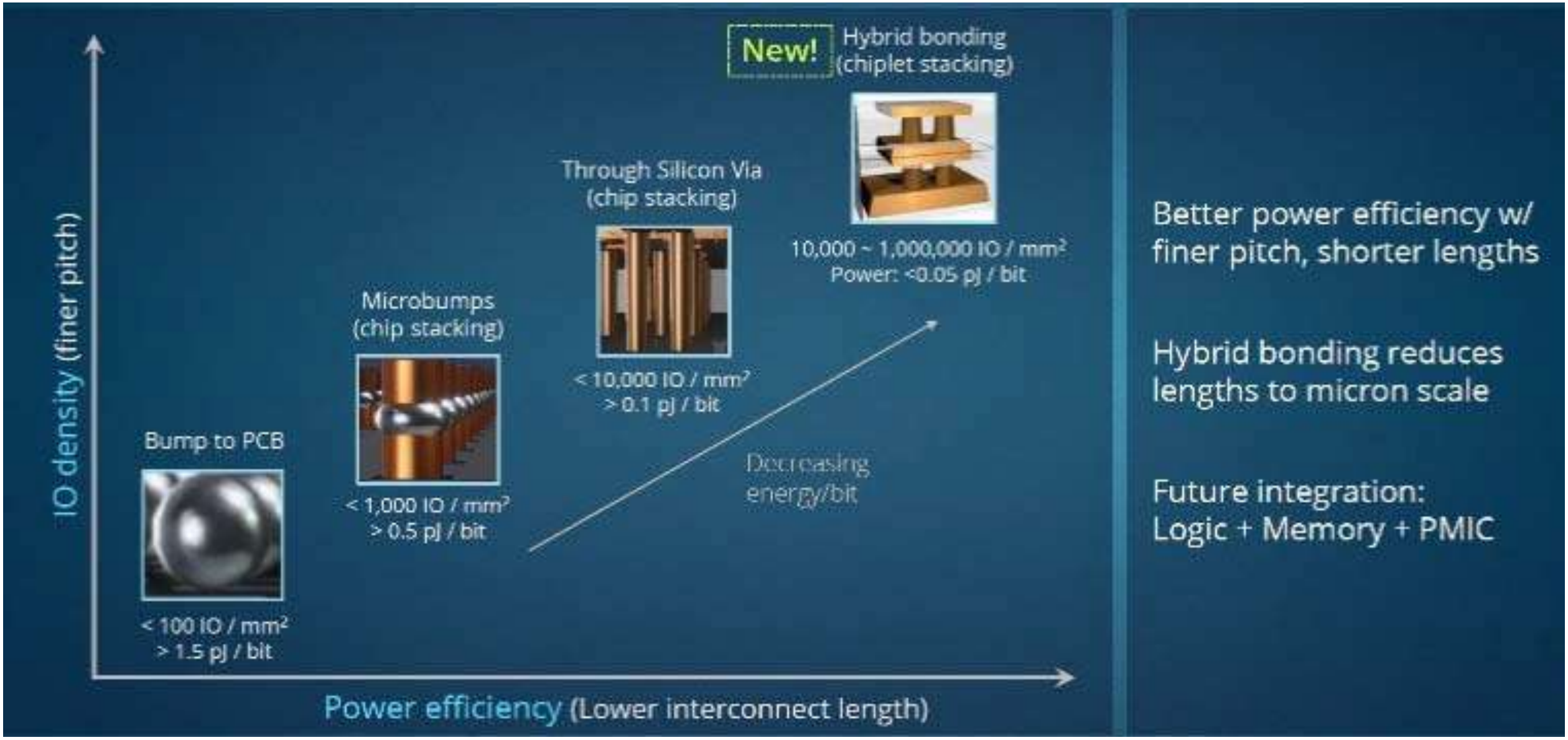
https://www.tomshardware.com/news/imec-reveals-sub-1nm-transistor-roadmap-3d-stacked-cmos-20-plans

ITF WORLD



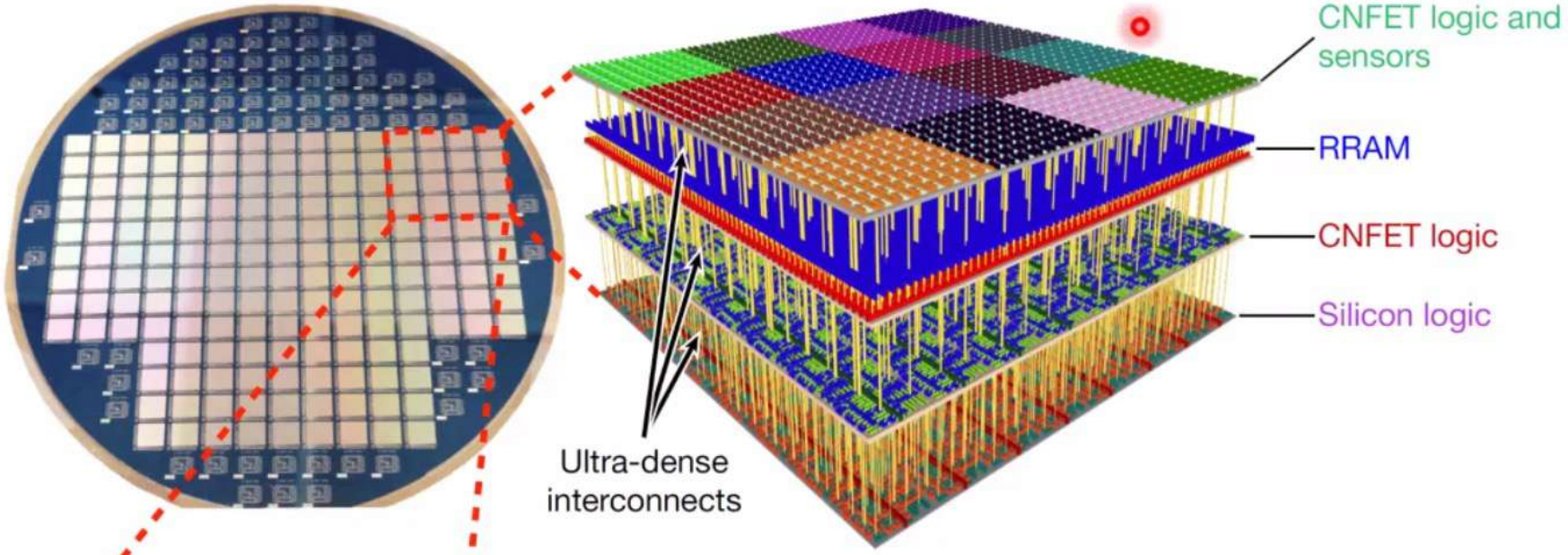
Sources: Companies, conference reports and IC Insights

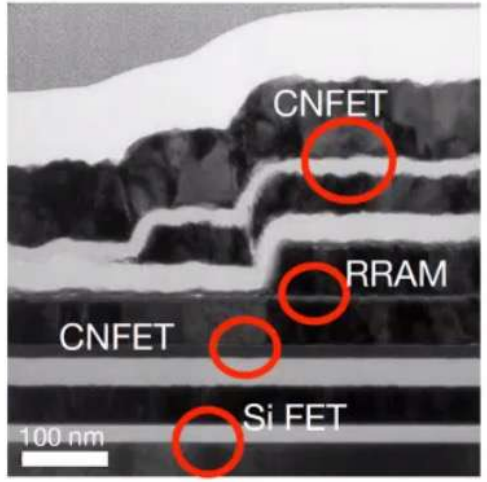
System interconnect roadmap of advanced packaging, with hybrid bonding as a new key enabler

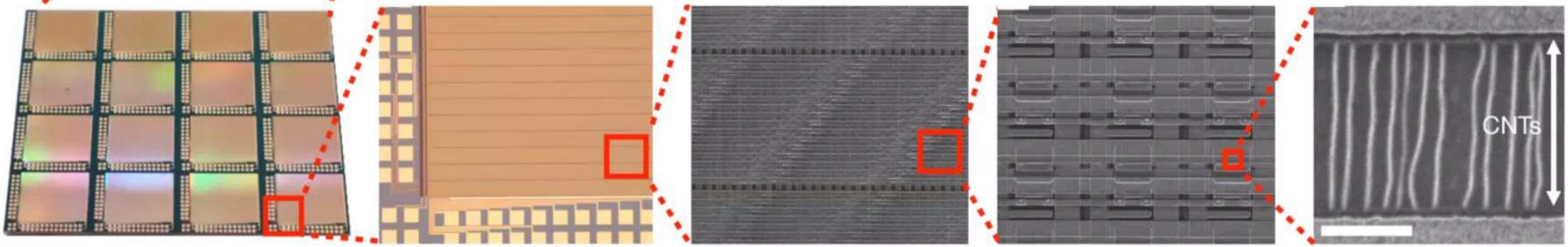


N3XT NANOSYSTEM

> 2 MILLION CNFETS, 1 MBIT RRAM

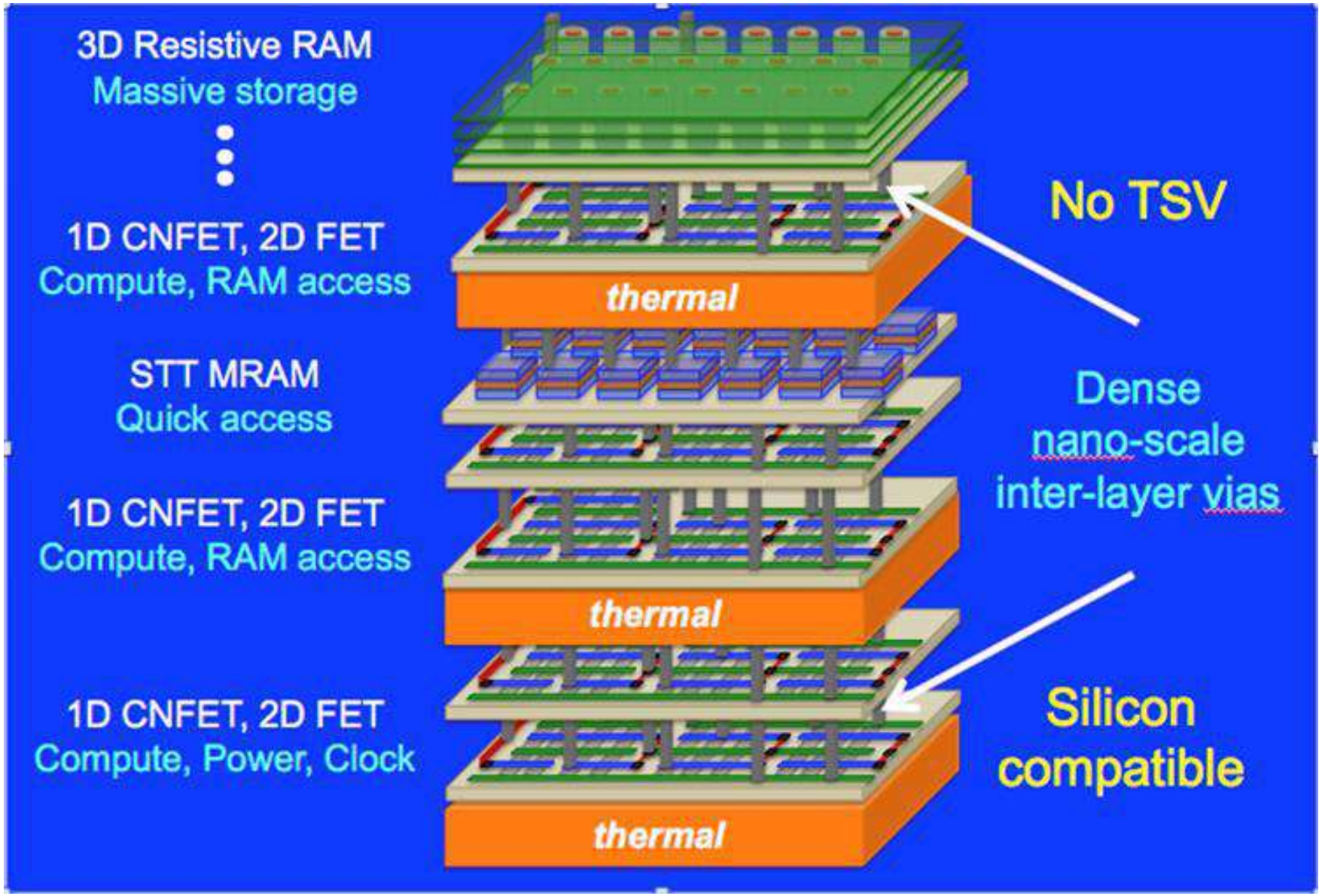






M. Shulaker,...H.-S. P. Wong, S. Mitra (Stanford), *Nature*, 2017

Planning for the advent of monolithic heterogeneous integration



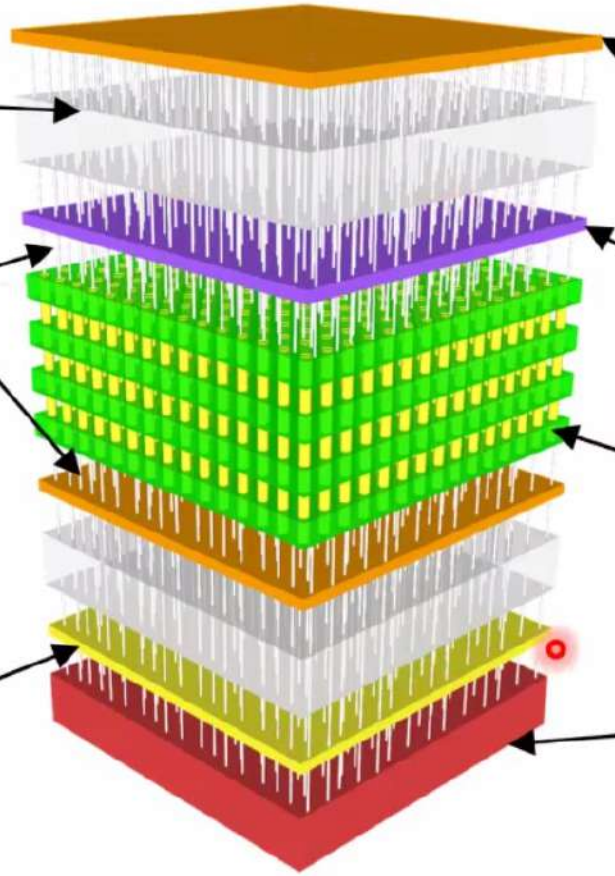
N3XT CHIP

ULT = upper layer transistor

Thermal management

Ultra-dense 3D vertical connectivity
(e.g., monolithic Inter-Layer Vias, ILVs)

ULT for memory cells
(e.g. Oxide semi. FETs for gain cell memory)



ULT logic for computing
(e.g. CNFETs)

ULT for memory access
(e.g. 2D FETs)

Dense memory
(e.g. 3D-VRRAM)

Si logic (e.g. FinFET)

The Different Ages of Scaling

(Different methods for different times)

1 Geometrical Scaling (1975-2002)

- Reduction of horizontal and vertical physical dimensions in conjunction with improved performance of planar transistors

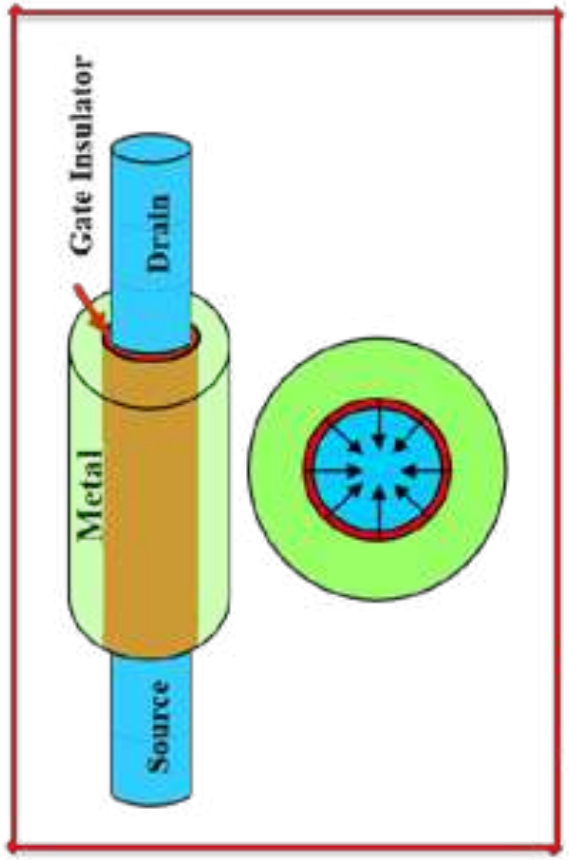
2 Equivalent Scaling (2003~2024)

- Reduction of only horizontal dimensions in conjunction with introduction of new materials and new physical effects. New vertical structures replace the planar transistor

3 3D Power Scaling (2025~2040)

- Transition to complete vertical device structures. Heterogeneous integration in conjunction with reduced power consumption become the technology drivers

The Ideal 3D MOS Transistor (2025~2040)



Fully Surrounding Metal Electrode

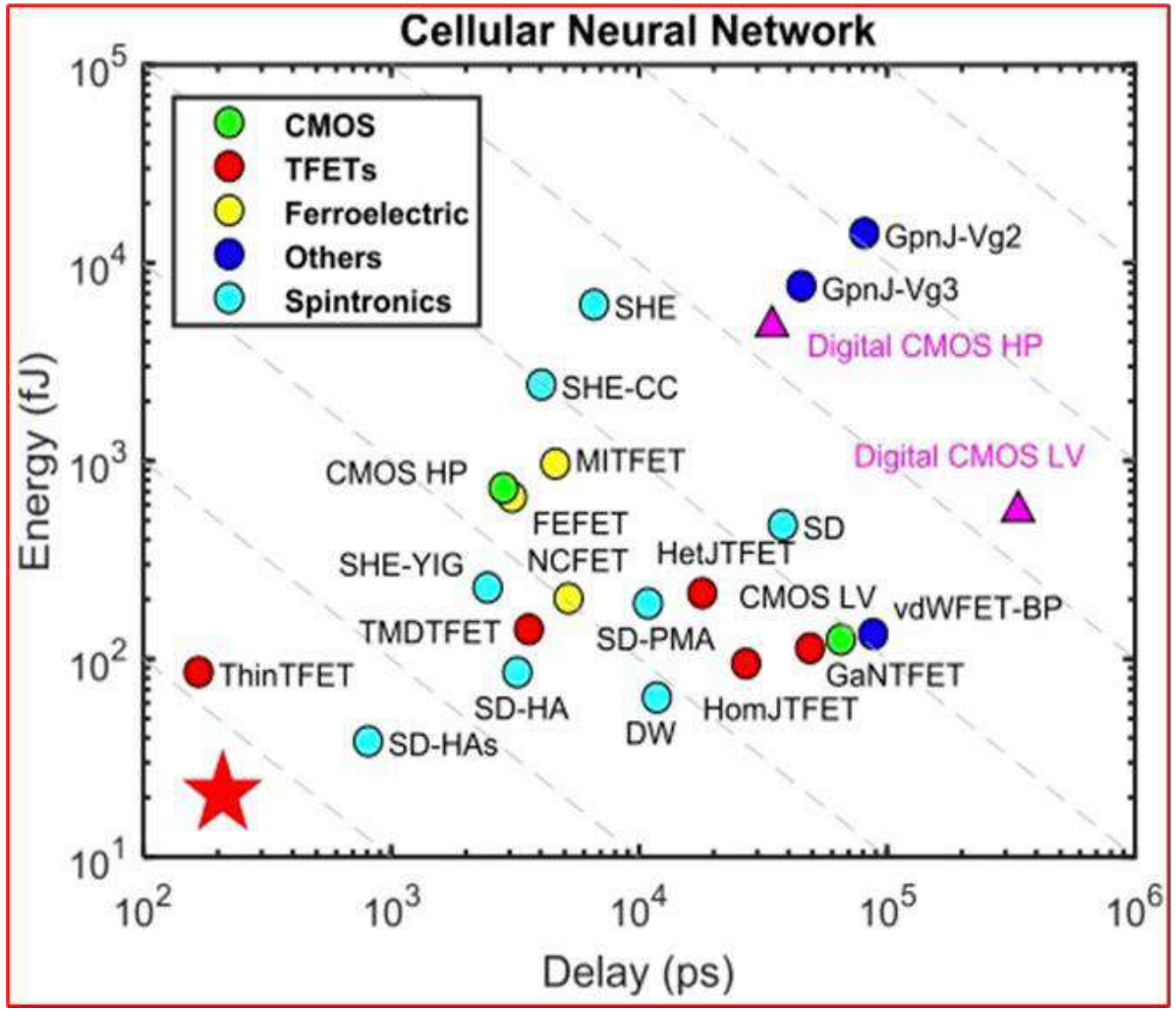
Fully Enclosed, Depleted Semiconductor

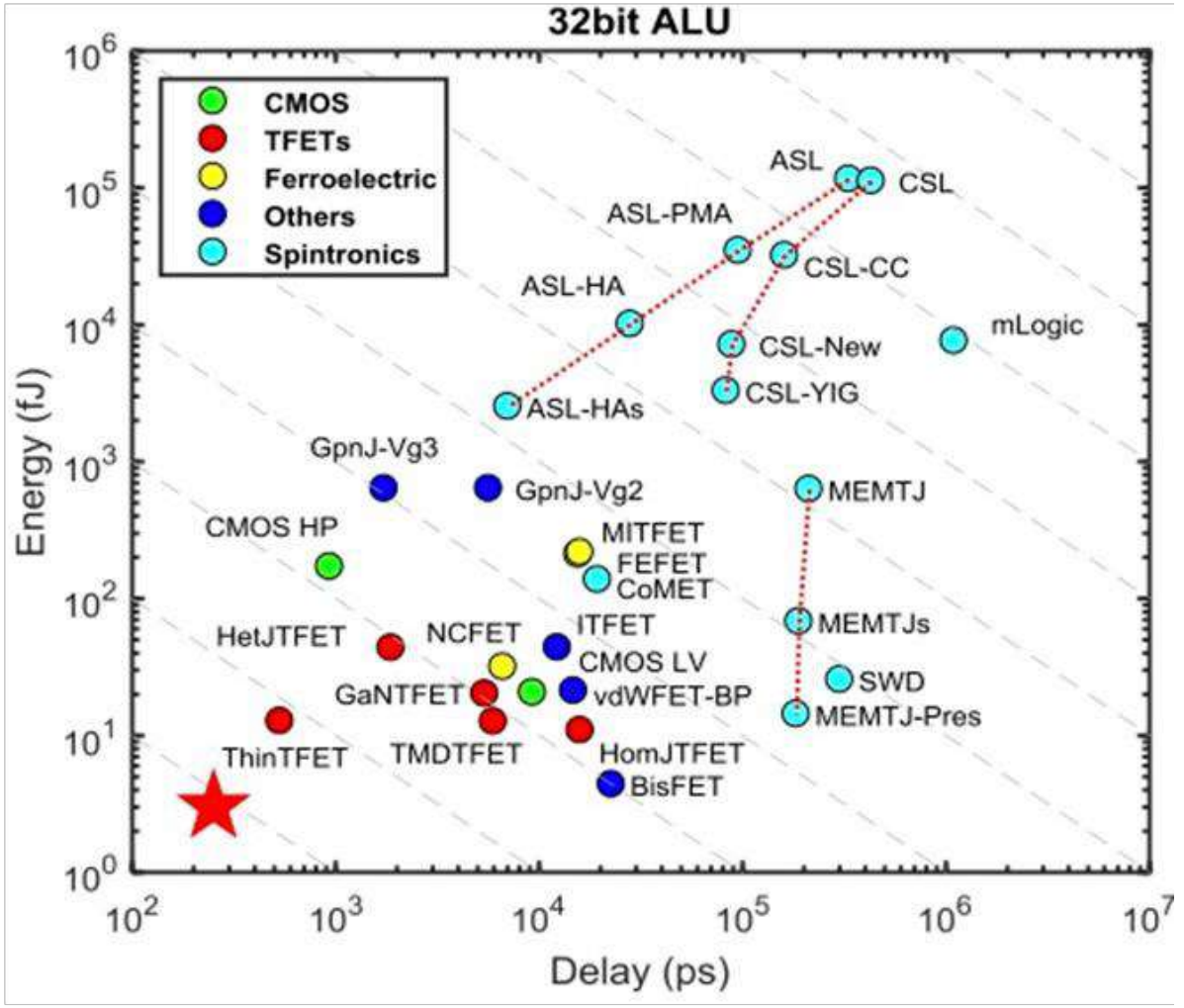
High-K Gate Insulator

Low Resistance Source/Drain

Band Engineered Semiconductor

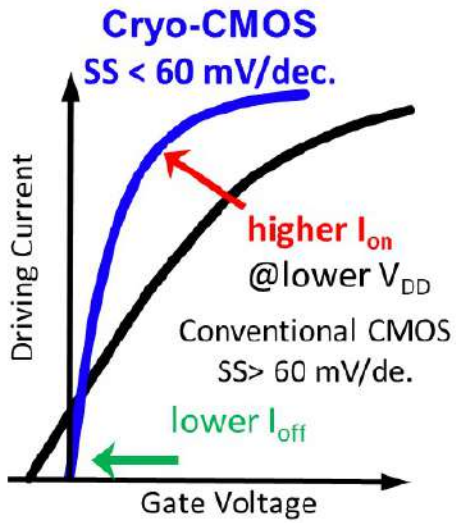
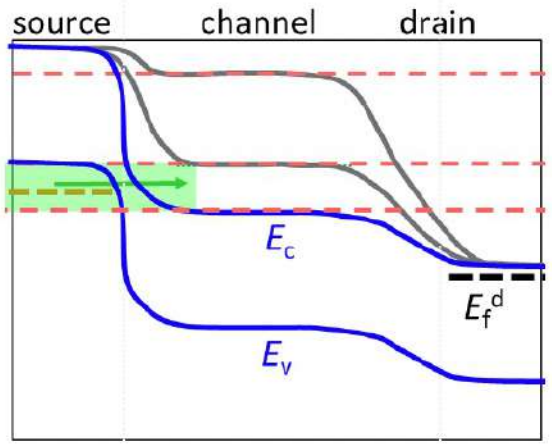
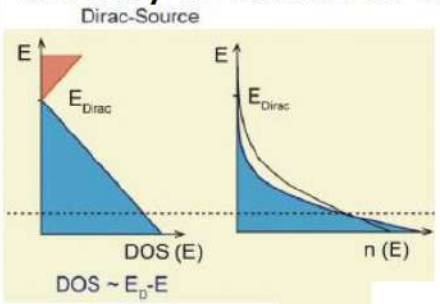
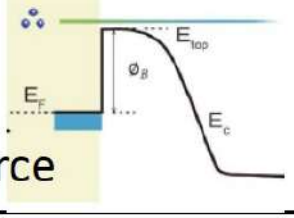
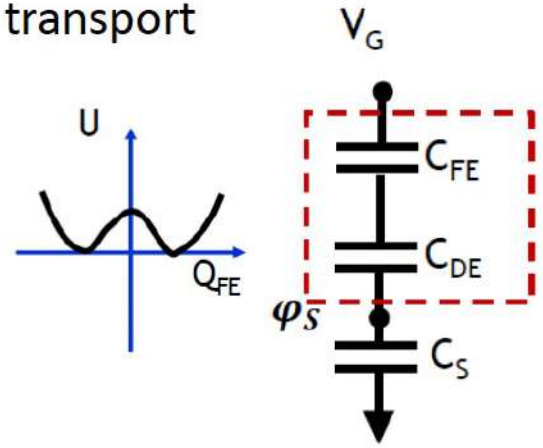
TFET Performance is Moving Close to the Target!



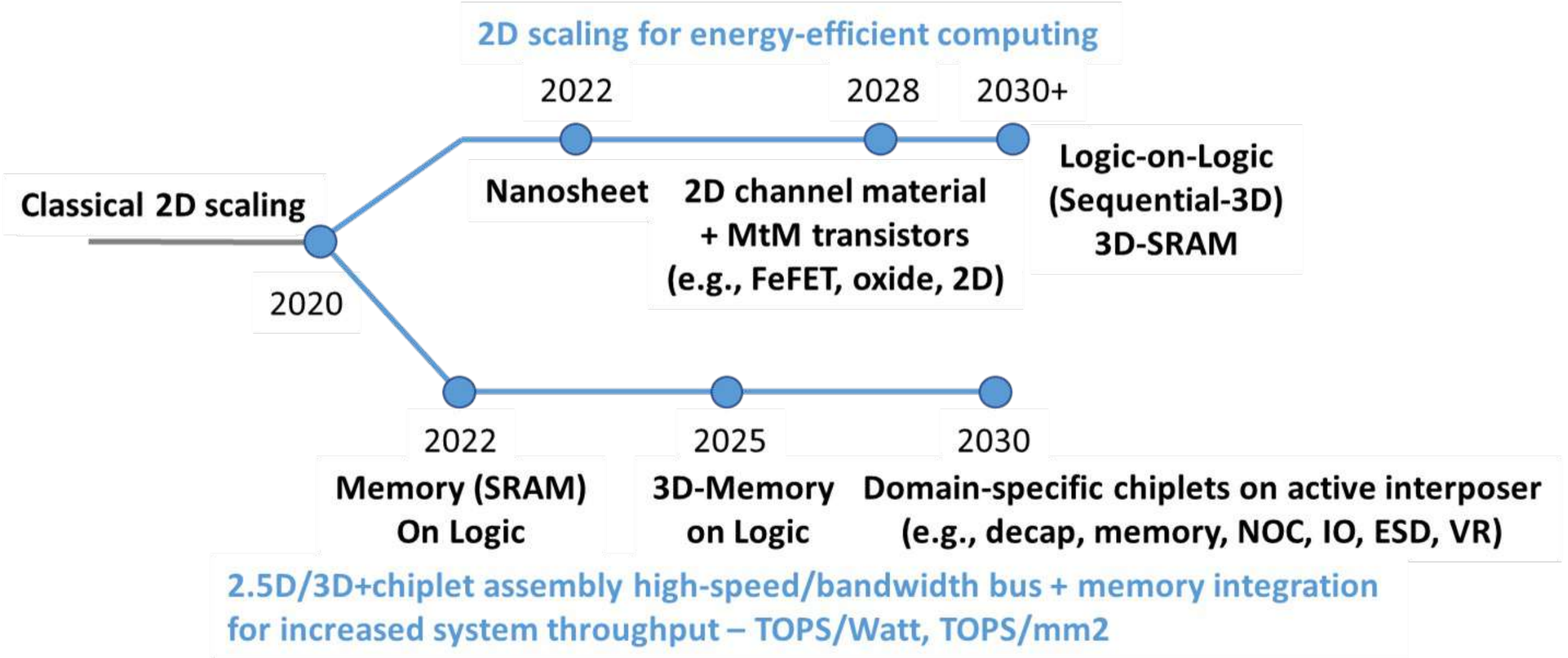


Beyond CMOS continues to improve towards goal!

Reducing supply voltage—Steep subthreshold swing

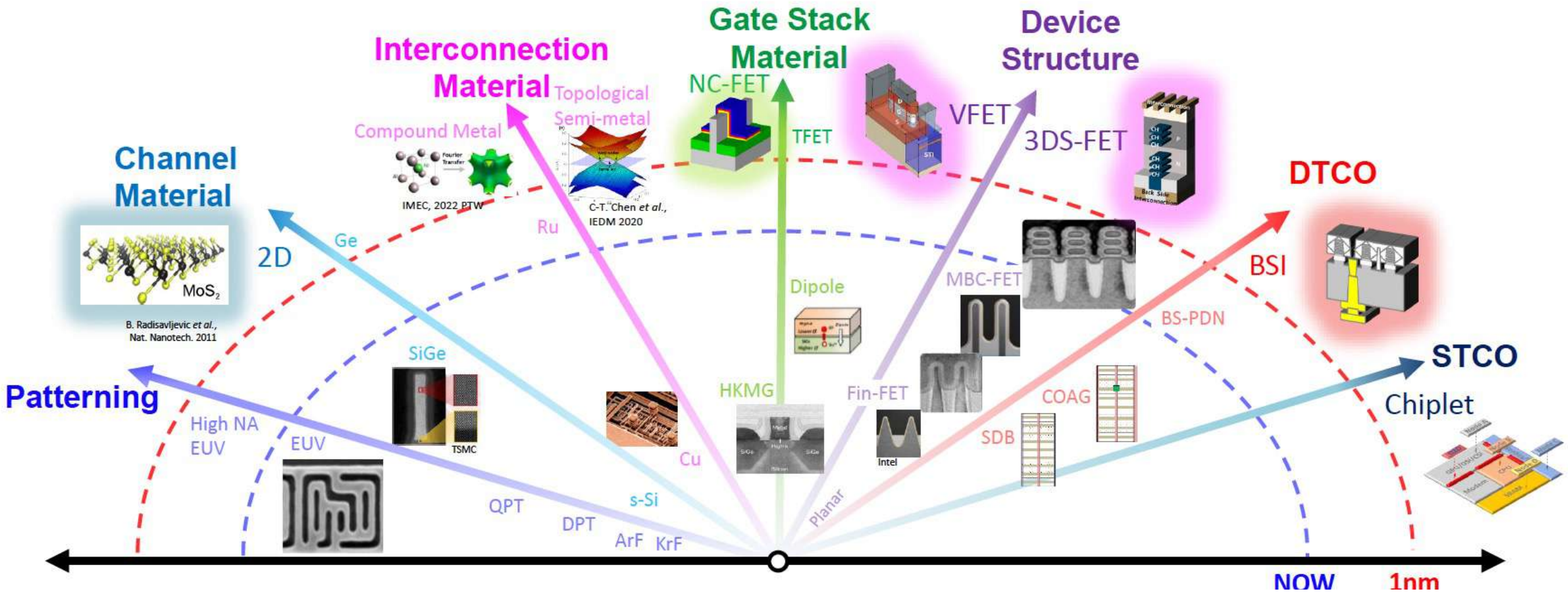
concept	CryoCMOS	Tunnel FET	Dirac / cold source FET	Negative capacitance
mechanism	$SS \propto {k_B T}/{q}$ 	Energy filtering by band to band tunneling around the Fermi level 	Energy filtering by limited density of states in source   Graphene used as source	Amplify internal potential with ferroelectric in gate stack without impacting transport 
challenge	External refrigeration Significant development needed	Low current Variability SS limited by TAT	Low current Same challenges as 2Ds	Stabilization Ultra-thin ferroelectric

2 complementing routes for More Moore scaling



Candidates for Energy Efficient CMOS Devices

" Innovations in structures, materials & processes to shrink standard cell area without decreasing effective device width & minimum metal width "



NSTC 國家科學及技術委員會
National Science and Technology Council

Emerging Semiconductor Heterogeneous Integration

- **Next-Generation Compound Semiconductor Project (2022-2025)**

B5G/6G High Frequency Semiconductor Technologies

⇨ **GaN** and **InP** compound semiconductor devices and circuits

Wide Bandgap High Power Semiconductor Technologies

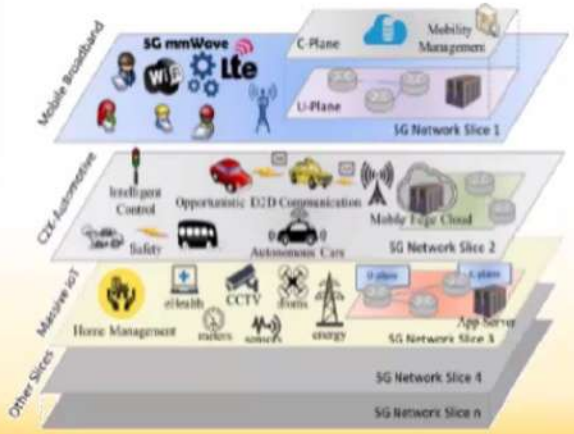
⇨ **GaN**, **SiC** based wide bandgap devices and circuits

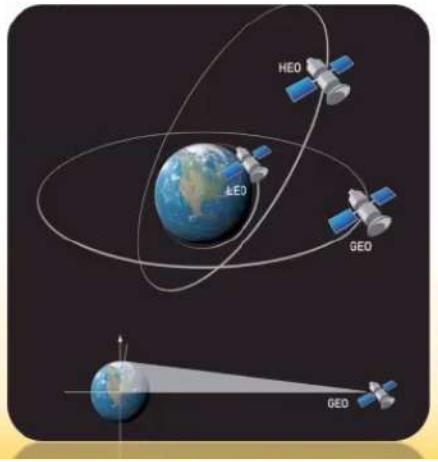
- **B5G/6G Prospective Technology Developments (2021-2024)**

– Sub-THz / THz technology

– Low-Earth Orbit (LEO) communications

– B5G/6G electromagnetic technology

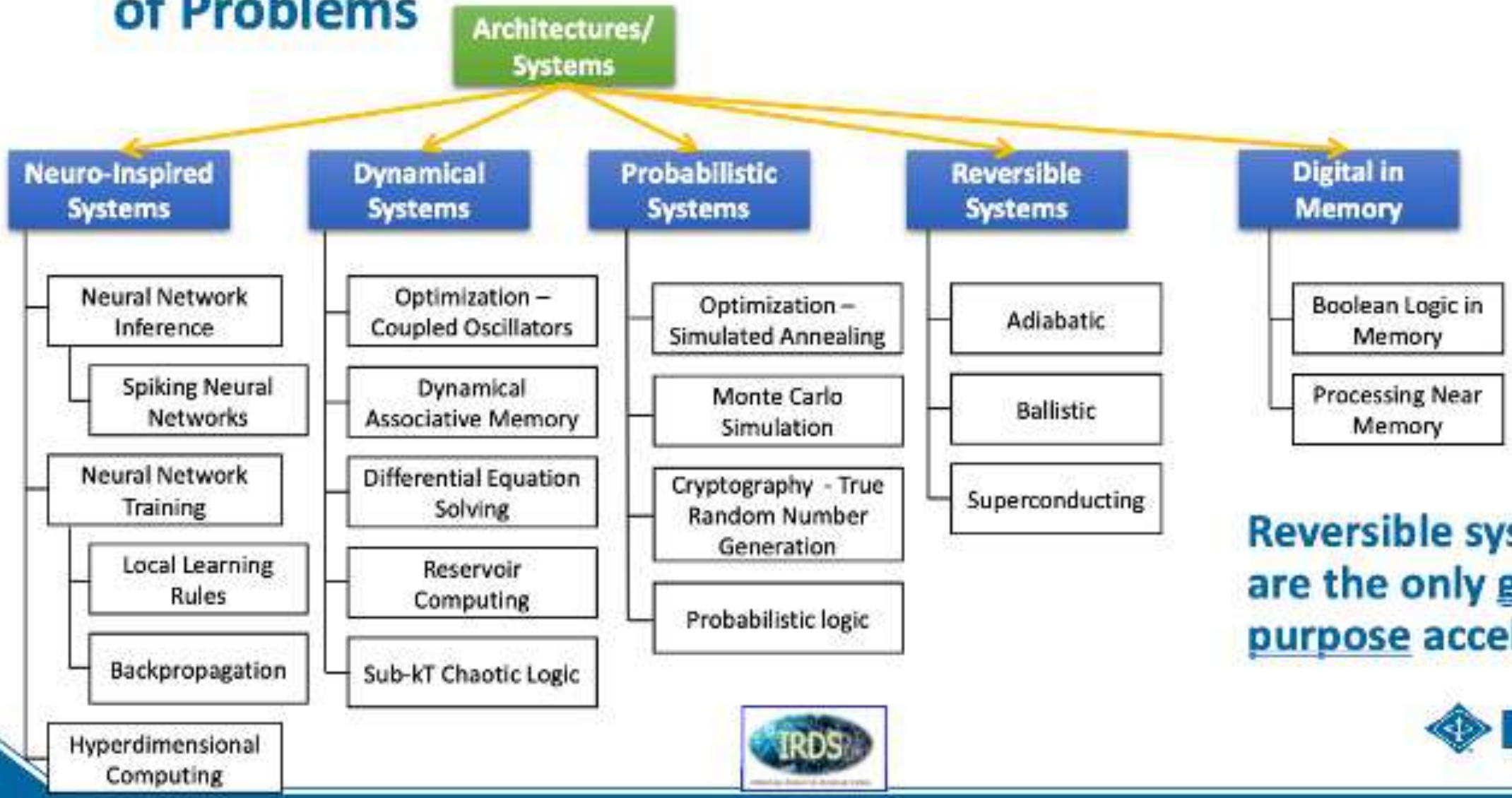




Wide-Bandgap Semiconductors (SiC, and GaN) for Power Applications

Image Courtesy: Infineon

Most Emerging Systems Accelerate a Particular Class of Problems

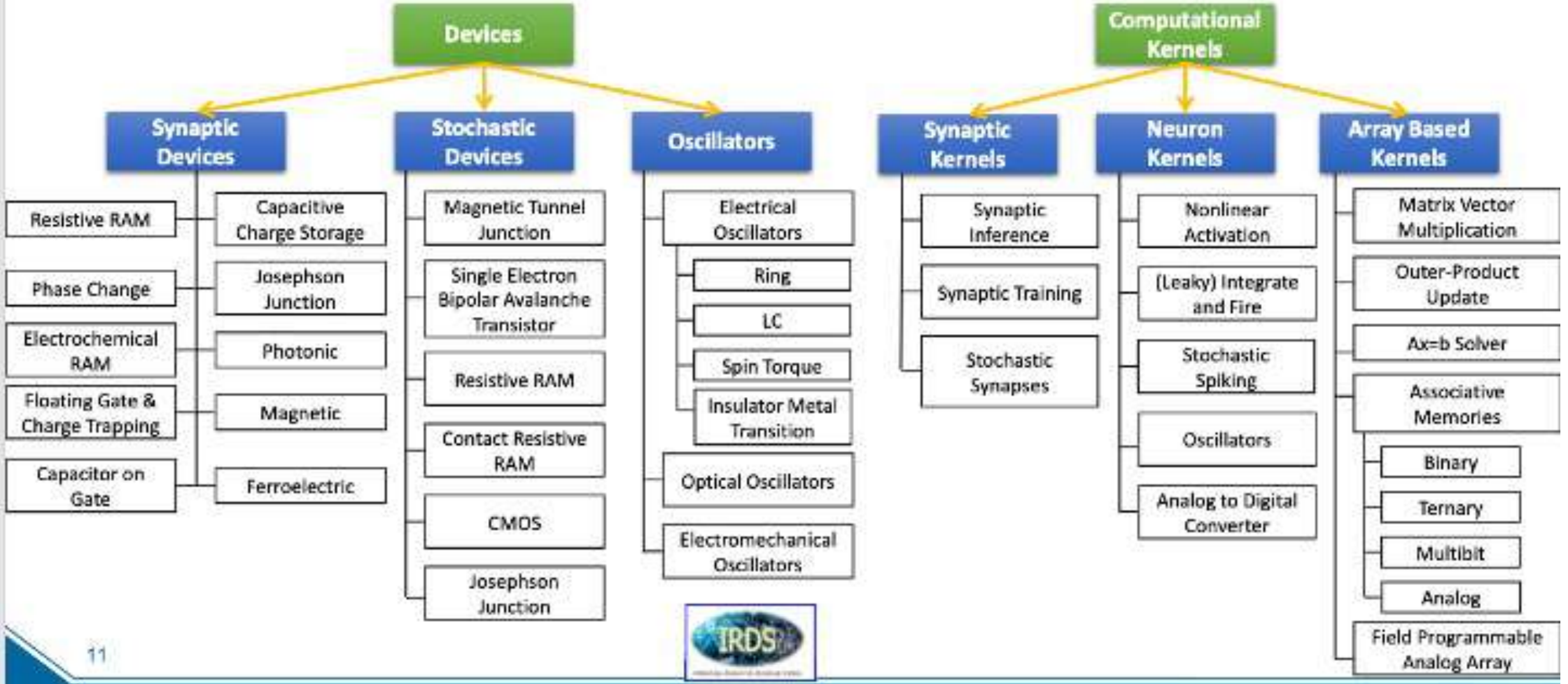


Reversible systems are the only general purpose accelerator

IRDS

IEEE

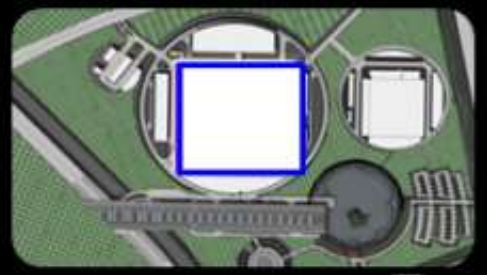
Emerging Devices → Emerging Kernels → Emerging Systems



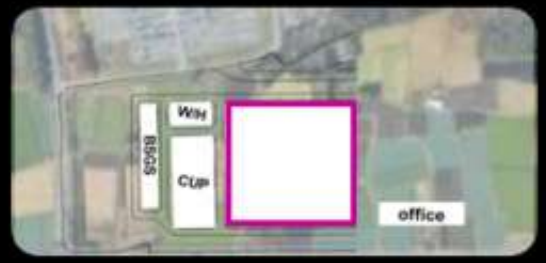
Expanding Global Footprint for 12” Fabs

Unleash Innovation

Fab16 - *Nanjing*



Fab23 - *Kumamoto*



China

Japan

US

Fab21 - *Arizona*

In production

Under construction during 2023

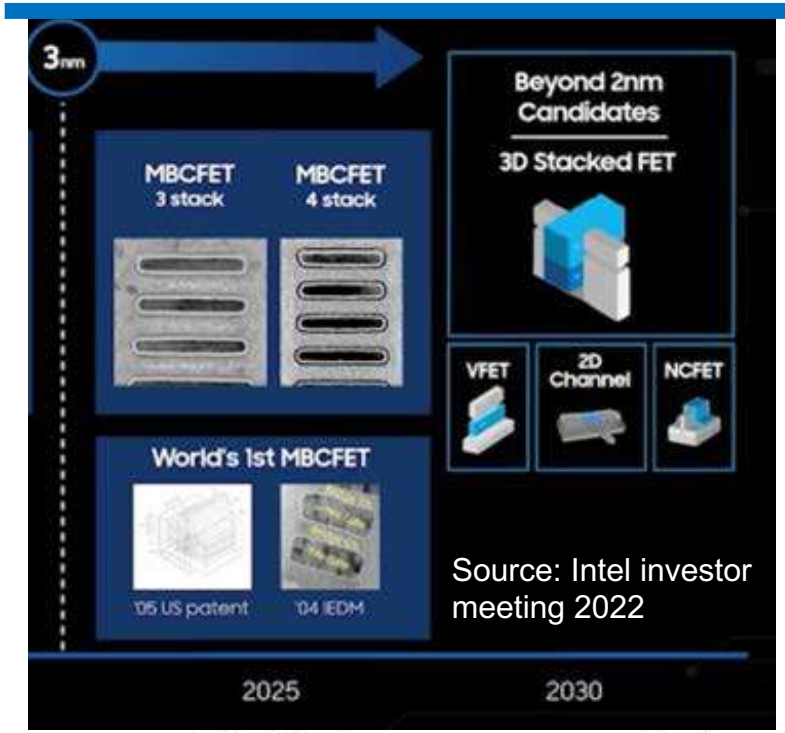
https://semiwiki.com/semiconductor-manufacturers/tsmc/328180-tsmc-2023-north-america-technology-symposium-overview-part-5/

https://commons.wikimedia.org/wiki/File:Intel_Worldwide_Manufacturing_Network.jpg

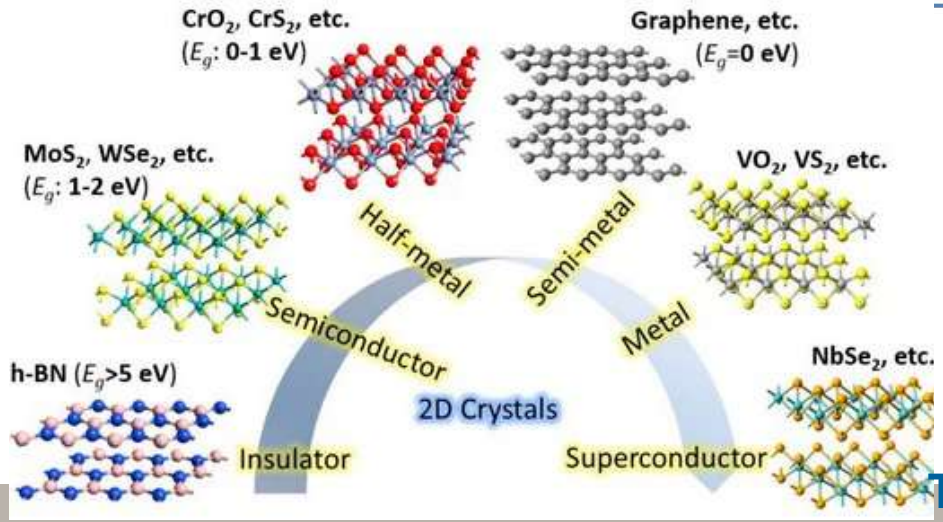
Agenda

- Introduction
- Semiconductor R&D Trends
- Transistor Scaling
- Materials and Devices
- Brief Introduction of Other Research Areas in My Group

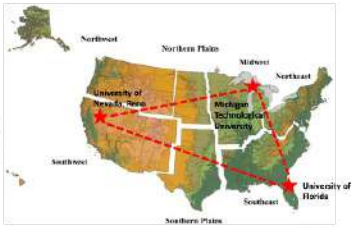
Energy-efficiency and Performance Innovation of Chips with 2-Dimensional Materials (EPIC 2-D Materials)



Source: Intel investor meeting 2022



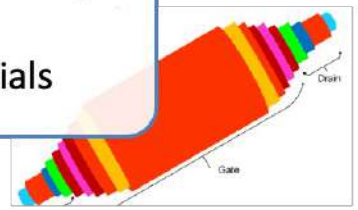
FuSe: EPIC-2D Materials



R1-EPSCoR State

CHIP (UNR)

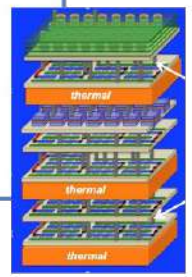
- Single Chip
- More than Moore (NCFET, TFET)
- 2D Materials



Well-resourced R1 Research

Interconnects (UF)

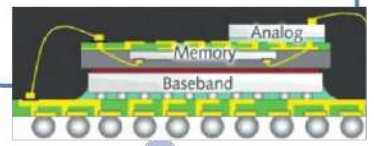
- Metaconductors
- Novel Interconnector materials



Carnegie R2 Research

Package (MTU)

- System in a Package (SiP)
- Several chips in one package



Engineering Education (UF)

Well-resourced R1 Research

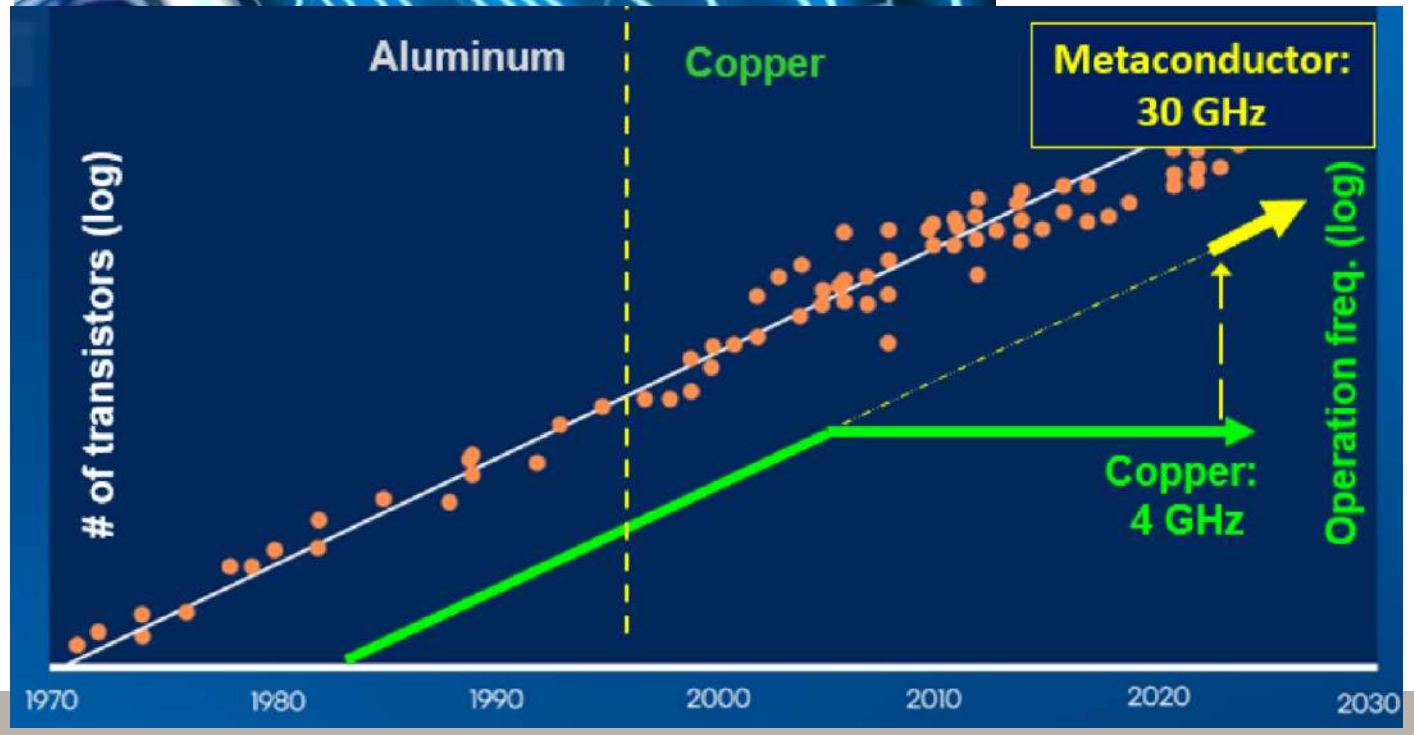
5

Transistor 2003-2025 evolution: From 2D Equivalent scaling to 3D Power scaling

Energy-efficient MetaConductors for Convergence of Sustainable Electronics (E-MC2 of Sustainable Electronics): $750k (Phase I Y1), $5M (Target Y2-Y3)

Revolutionizing the Semiconductor Industry

Our **metaconductors** help the electronics industry achieve high performance computing with 200% power efficiency improvement.



Jin W. Choi
(ECE, MTU)

Jeongwon Park
(EBE, **UNR**)

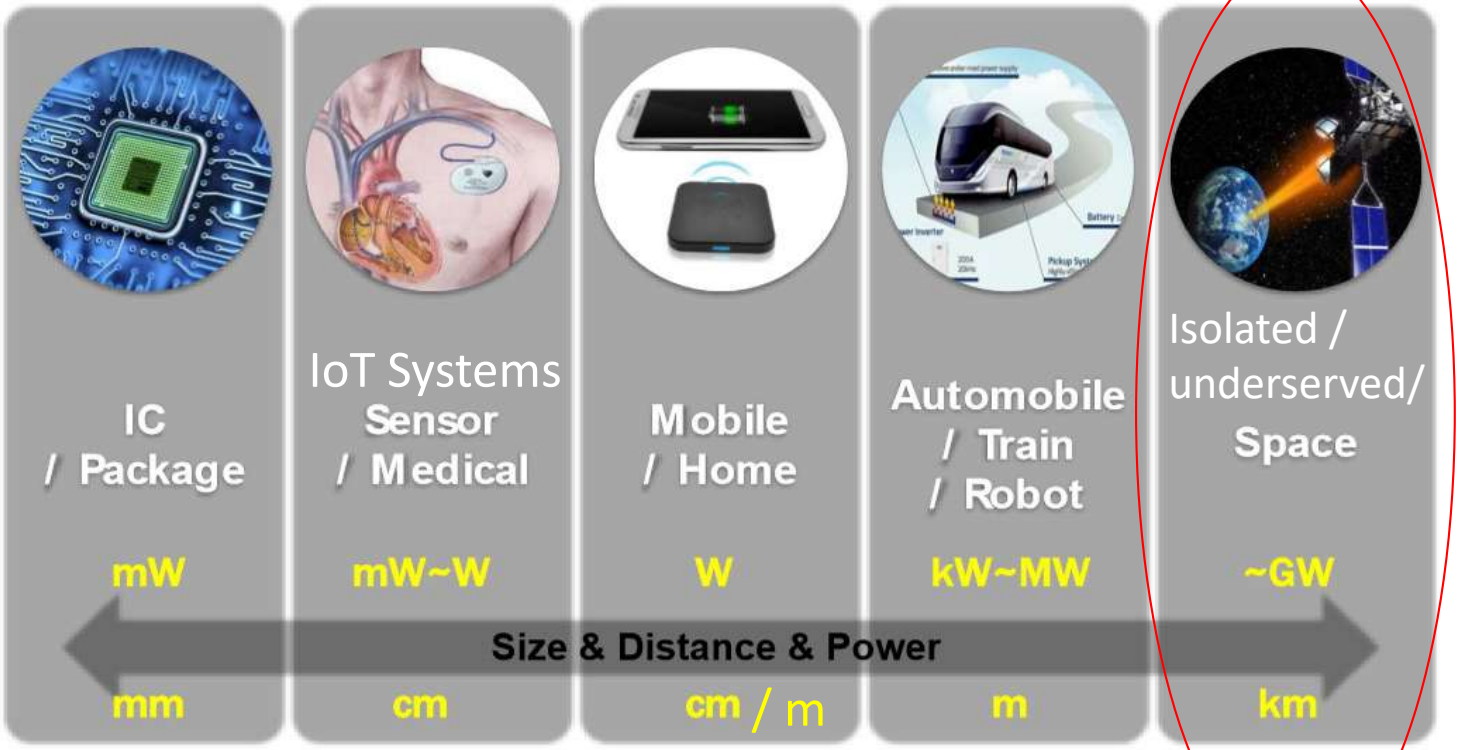
Gloria Kim
(EED, UF)

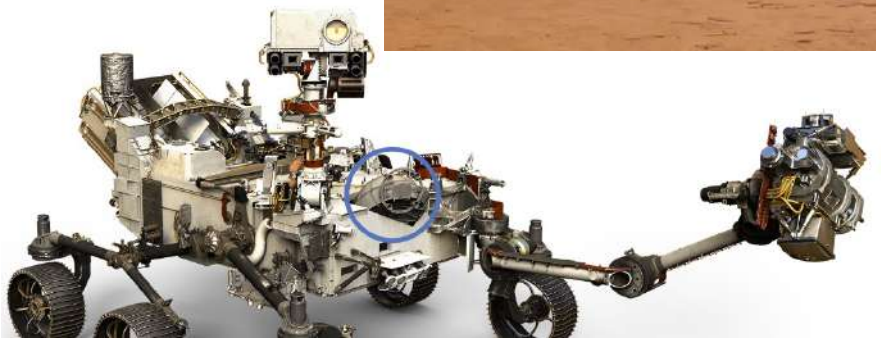
PI: YK Yoon
(ECE, UF)

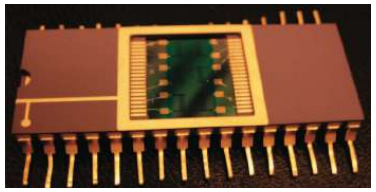
Meta-Research Triangle

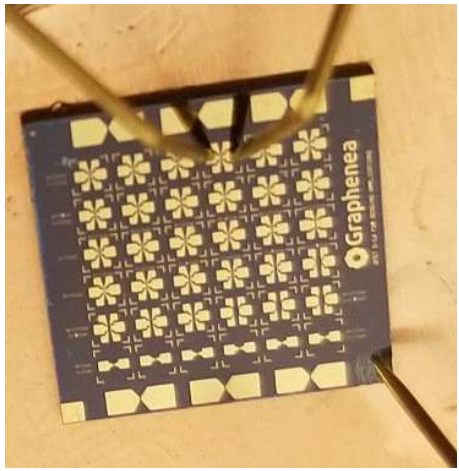
Wireless Power Transfer

Multiscale





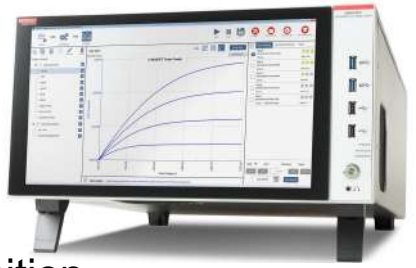


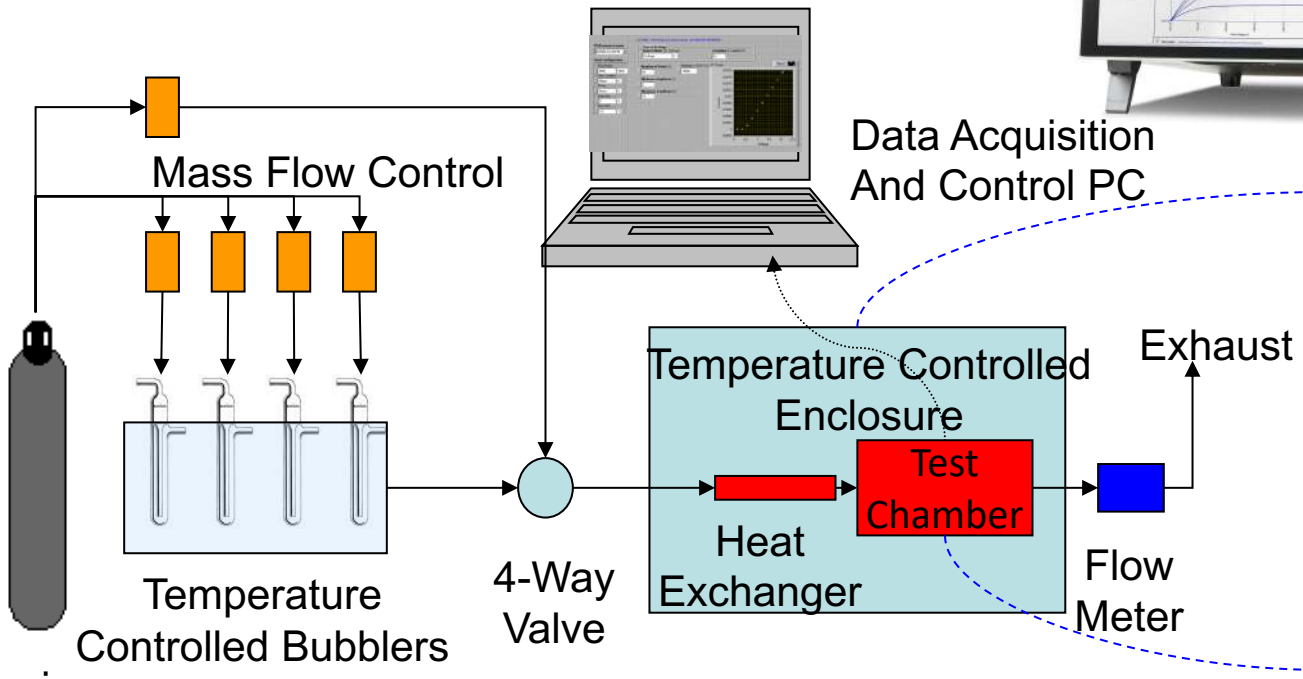


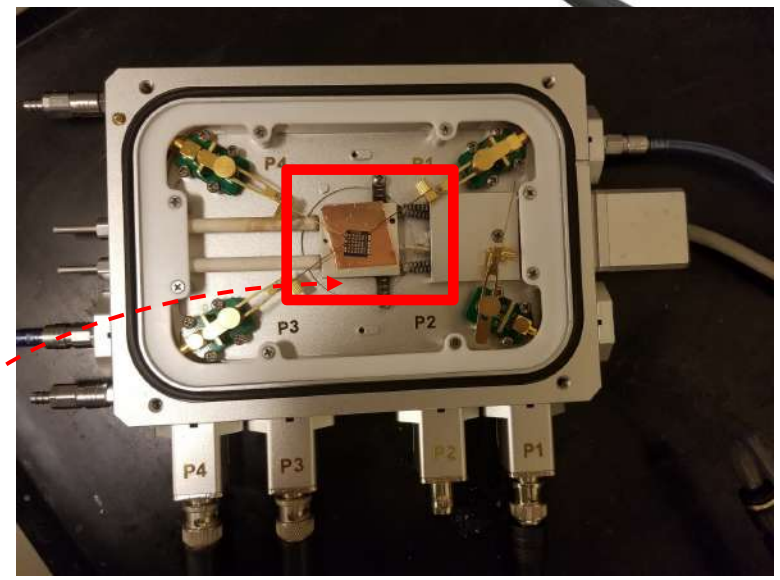
NASA

NSF

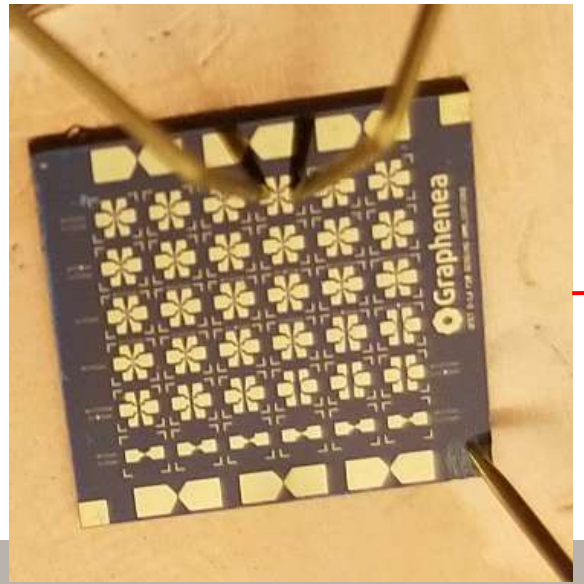
Evaluation and Sensor Performance







Frame Dimensions: 180mm × 130mm × 27mm

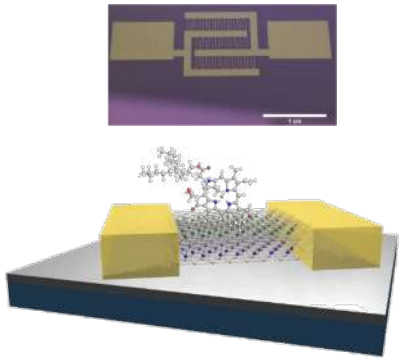


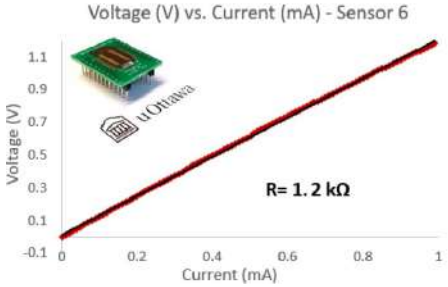
Test sensors for ppb sensitivity and selectivity
Temperature range: -190 °C to 600 °C

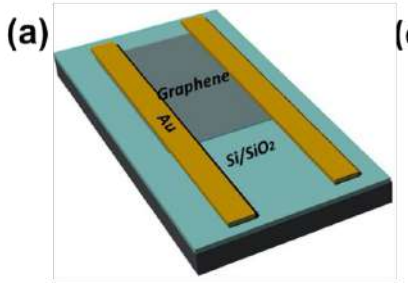
HORIBA

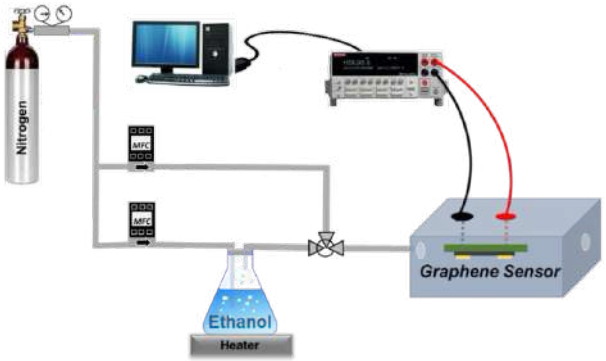
Sensitive detection and identification of airborne chemicals and biological agents

- *2D materials FET response in different environments*

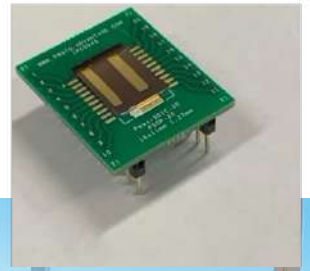




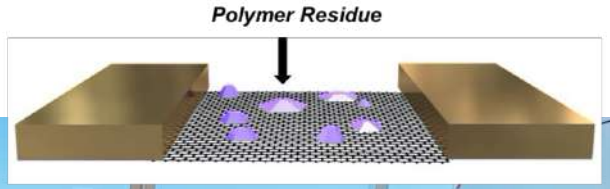




(b)

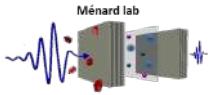


(d)



- *Light matter interaction for selectivity*

Ménard lab



- *Device miniaturization, connectivity, packaging etc.*

Park Lab @uOttawa

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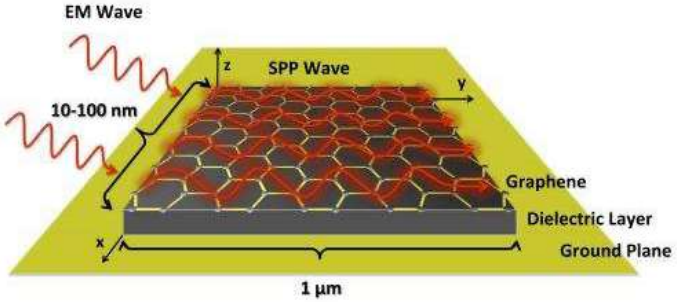
INNOVATION POUR LA DÉFENSE, L'EXCELLENCE ET LA SÉCURITÉ

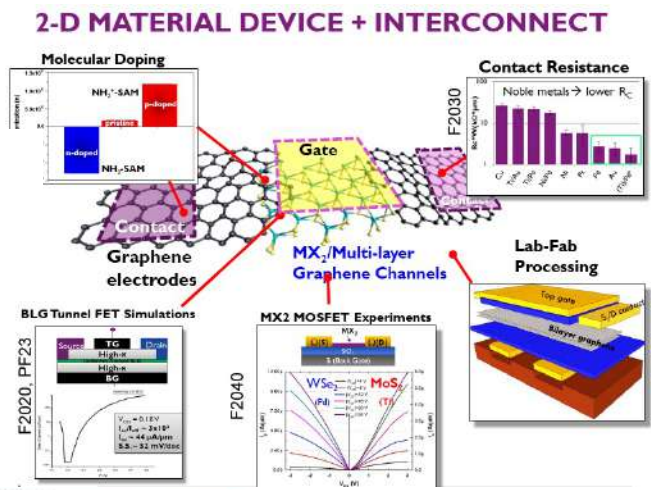
ACS Appl. Mater. Interfaces 2020

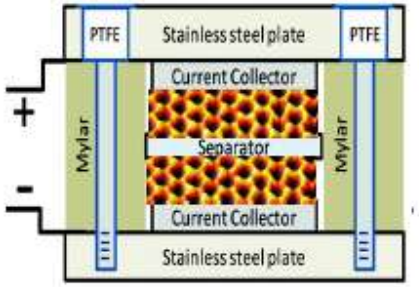
Graphene Roadmap



Antennas

High-Performance Computing



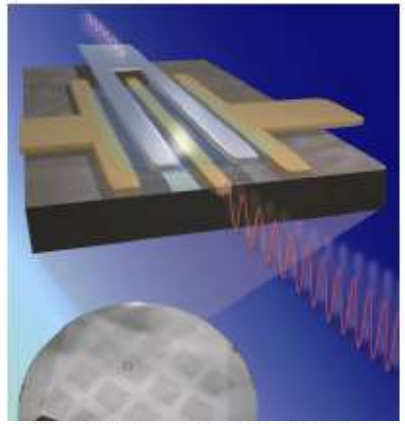


Supercapacitors

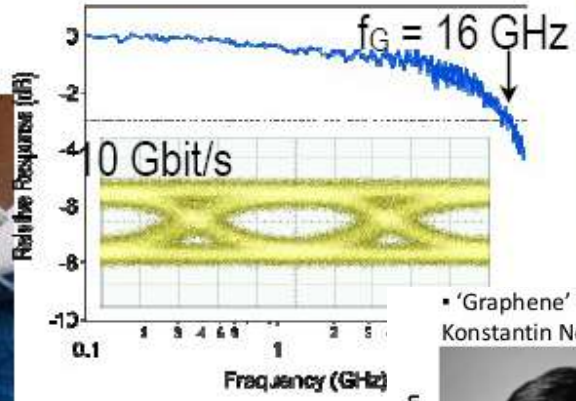
Processing Challenges

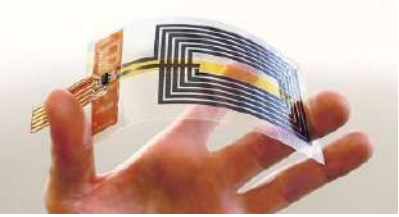
Low-cost RF Circuits
Mid-performance (GHz)

Optoelectronics Devices



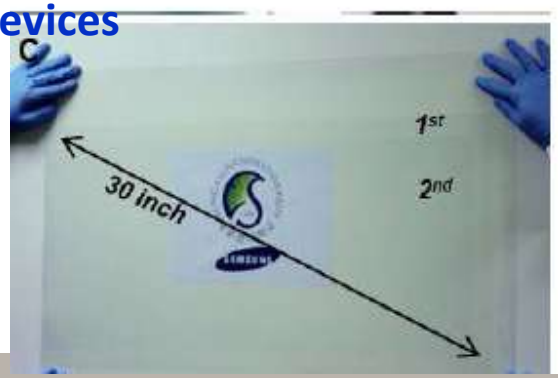
Smart Sensors





Flexible antennas in consumer electronic devices

Transparent electrodes



▪ 'Graphene' was first isolated in the lab by Professor Andre Geim with former student Konstantin Novoselov at the University of Manchester, England in 2004

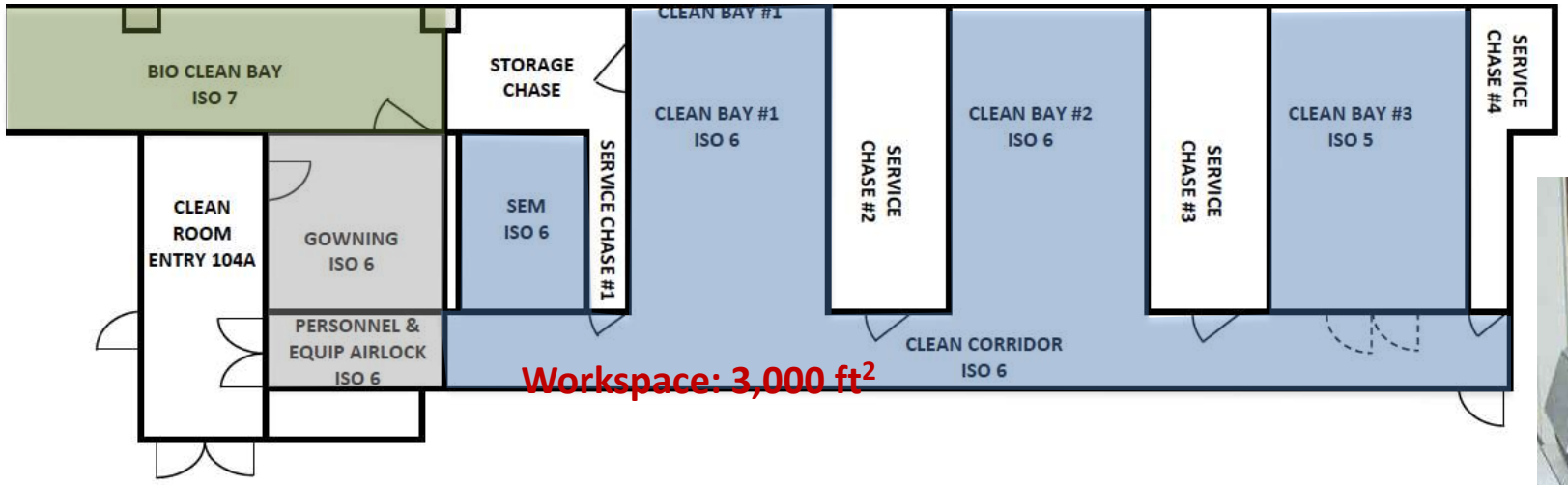
Pr. Andre K. Geim

2010 Nobel Prize

for "groundbreaking experiments regarding the two-dimensional material graphene"
(Both were later Knighted, twice)

Pr. Kostya Novoselov

Davidson Foundation Cleanroom



Workspace: 3,000 ft^2

Mask aligner

CVD: 2D Materials

E-beam evaporator

Image Source: University of Nevada, Reno

Thank you for your support

University of Nevada, Reno

uOttawa

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KOREA ELECTROTECHNOLOGY RESEARCH INSTITUTE

NASA

AIR FORCE RESEARCH LABORATORY

APPLIED MATERIALS

DARPA

UNIVERSITY OF CALIFORNIA · SAN DIEGO

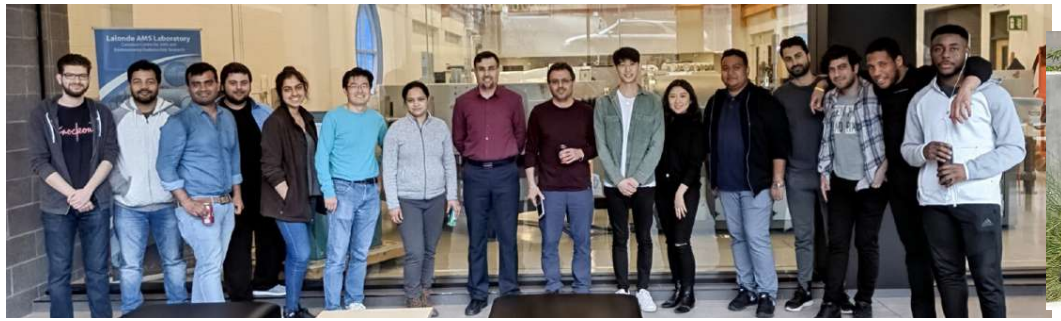
Stanford University

SLAC
NATIONAL ACCELERATOR LABORATORY

NSERC
CRSNG

BERKELEY LAB
LAWRENCE BERKELEY NATIONAL LABORATORY

Santa Clara University



University of Nevada, Reno